Virtex-5 FPGA ML550 Networking Interfaces Platform

User Guide

UG202 (v1.4) April 18, 2008

XILINX®

Revision History

The following table shows the revision history for this document.

Date	Version	Revision
05/12/06	1.0	Initial Xilinx release.
04/02/07	1.1	Revised User Guide with LXT and SXT devices. Added reference to Power Monitor header in Figure 1-1, page 13. Added note to Table 3-2, page 21. Changed fuse in Figure 3-7, page 29. Added “Power Monitor Connector” section. Revised LVDS_DATAOUT_1, Pin 47 and Pin 49, in Table A-1, page 51. Revised LVDS_DATAOUT_43 in Table A-3, page 54.
06/22/07	1.2	Updated pin numbers in Table 3-12, page 33. Added Appendix D, “ML550 Starter UCF.”
10/08/07	1.3	Updated pin names/numbers in Table A-1, Table A-2, and Table A-4.
04/18/08	1.4	Added new section “ML550 System Monitor and Power Monitor Support,” page 34 to Chapter 3.

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Appendix D: ML550 Starter UCF

About This Guide

This user guide is a description of the Virtex®-5 FPGA ML550 Networking Interfaces Development Board. Complete and up-to-date documentation of the Virtex-5 family of FPGAs is available on the Xilinx website at http://www.xilinx.com/virtex5.

Guide Contents

This manual contains the following chapters:

- Chapter 1, "Introduction"
- Chapter 2, "Getting Started"
- Chapter 3, "Hardware Description"
- Chapter 4, "Configuration"
- Appendix A, "LVDS"
- Appendix B, "LVDS Loopback Board"
- Appendix C, "LCD Interface"
- Appendix D, "ML550 Starter UCF"

Additional Documentation

The following documents are also available for download at http://www.xilinx.com/virtex5.

- Virtex-5 Family Overview

  The features and product selection of the Virtex-5 family are outlined in this overview.

- Virtex-5 FPGA Data Sheet: DC and Switching Characteristics

  This data sheet contains the DC and Switching Characteristic specifications for the Virtex-5 family.

- Virtex-5 FPGA User Guide

  Chapters in this guide cover the following topics:

  - Clocking Resources
  - Clock Management Technology (CMT)
  - Phase-Locked Loops (PLLs)
  - Block RAM
  - Configurable Logic Blocks (CLBs)
  - SelectIO™ Resources

  - SelectIO Logic Resources
  - Advanced SelectIO Logic Resources
- Virtex-5 FPGA RocketIO GTP Transceiver User Guide

  This guide describes the RocketIO™ GTP transceivers available in the Virtex-5 LXT and SXT platforms.
- Virtex-5 FPGA RocketIO GTX Transceiver User Guide

  This guide describes the RocketIO GTX transceivers available in the Virtex-5 FXT platform.
- Virtex-5 FPGA Embedded Processor Block for PowerPC® 440 Designs

  This reference guide is a description of the embedded processor block available in the Virtex-5 FXT platform.
- Virtex-5 FPGA Embedded Tri-Mode Ethernet MAC User Guide

  This guide describes the dedicated Tri-Mode Ethernet Media Access Controller available in the Virtex-5 LXT, SXT, and FXT platforms.
- Virtex-5 FPGA Integrated Endpoint Block User Guide for PCI Express Designs

  This guide describes the integrated Endpoint blocks in the Virtex-5 LXT, SXT, and FXT platforms used for PCI Express® designs.
- Virtex-5 FPGA XtremeDSP Design Considerations User Guide

  This guide describes the XtremeDSP™ slice and includes reference designs for using the DSP48E.
- Virtex-5 FPGA Configuration Guide

  This all-encompassing configuration guide includes chapters on configuration interfaces (serial and SelectMAP), bitstream encryption, Boundary-Scan and JTAG configuration, reconfiguration techniques, and readback through the SelectMAP and JTAG interfaces.
- Virtex-5 FPGA System Monitor User Guide

  The System Monitor functionality available in all the Virtex-5 devices is outlined in this guide.
- Virtex-5 FPGA Packaging and Pinout Specifications

  This specification includes the tables for device/package combinations and maximum I/Os, pin definitions, pinout tables, pinout diagrams, mechanical drawings, and thermal specifications.
- Virtex-5 FPGA PCB Designer's Guide

  This guide provides information on PCB design for Virtex-5 devices, with a focus on strategies for making design decisions at the PCB and interface level.

Additional Support Resources

To search the database of silicon and software questions and answers, or to create a technical support case in WebCase, see the Xilinx website at: http://www.xilinx.com/support.

Typographical Conventions

This document uses the following typographical conventions. An example illustrates each convention.

Convention	Meaning or Use	Example
Italic font	References to other documents	See the *Virtex-5 Configuration Guide* for more information.
	Emphasis in text	The address (F) is asserted *after* clock event 2.
Underlined Text	Indicates a link to a web page.	http://www.xilinx.com/virtex5

Online Document

The following conventions are used in this document:

Convention	Meaning or Use	Example
Blue text	Cross-reference link to a location in the current document	See the section "Additional Support Resources" for details. Refer to "Clock Generation" in Chapter 3 for details.
Red text	Cross-reference link to a location in another document	See Figure 2 in the *Virtex-5 Data Sheet*
Blue, underlined text	Hyperlink to a website (URL)	Go to http://www.xilinx.com for the latest documentation.

Chapter 1

Introduction

About the Virtex-5 FPGA Source-Synchronous Interfaces Tool Kit

The Virtex®-5 FPGA ML550 Source-Synchronous Interfaces Tool Kit provides a complete development platform for designing and verifying applications based on the Virtex-5 LXT FPGA family. This kit allows designers to implement high-speed applications with extreme flexibility using IP cores and customized modules. The Virtex-5 LXT FPGA, with its column-based architecture, makes it possible to develop highly flexible networking applications.

The Virtex-5 FPGA ML550 Source-Synchronous Interfaces Tool Kit includes the following:

- Virtex-5 FPGA ML550 Networking Interfaces Development Board (XC5VLX50T-FFG1136 FPGA)
- 5V/6.5 A DC power supply
- Country-specific power supply line cord
- USB B-to-A cable
- Xilinx® LVDS Loopback board PN 0431395
- Documentation and reference design CD-ROM

Optional items that also support development efforts include:

- Xilinx ISE® software
- JTAG cable or Xilinx Platform Cable USB

For assistance with any of these items, contact your local Xilinx distributor or visit the Xilinx online store at www.xilinx.com.

The heart of the Virtex-5 FPGA ML550 Source-Synchronous Interfaces Tool Kit is the ML550 Development Board. This manual provides comprehensive information on Rev 1 and later revisions of this board.

Virtex-5 FPGA ML550 Networking Interfaces Development Board

The ML550 Development Board includes the following:

- XC5VLX50T-FFG1136 FPGA
- 64M x 8 DDR SDRAM memory
- Eight clock sources:
  - 200 MHz, 250 MHz, 133 MHz, and 33 MHz on-board oscillators
  - Two ICS8442 clock synthesizer devices
  - Two sets of SMA differential clock input connectors
- One USB "B" port
- One 64 x 128 pixel LCD – Optional
- A System ACE™ CompactFlash (CF) Configuration Controller that allows storing and downloading of up to eight FPGA configuration image files
- Six Samtec LVDS connectors (a total of 53 differential input and 53 differential output channels)
- Onboard power regulators with ±5% output margin test capabilities, in 2.5% increments

Figure 1-1 shows the ML550 Development Board.

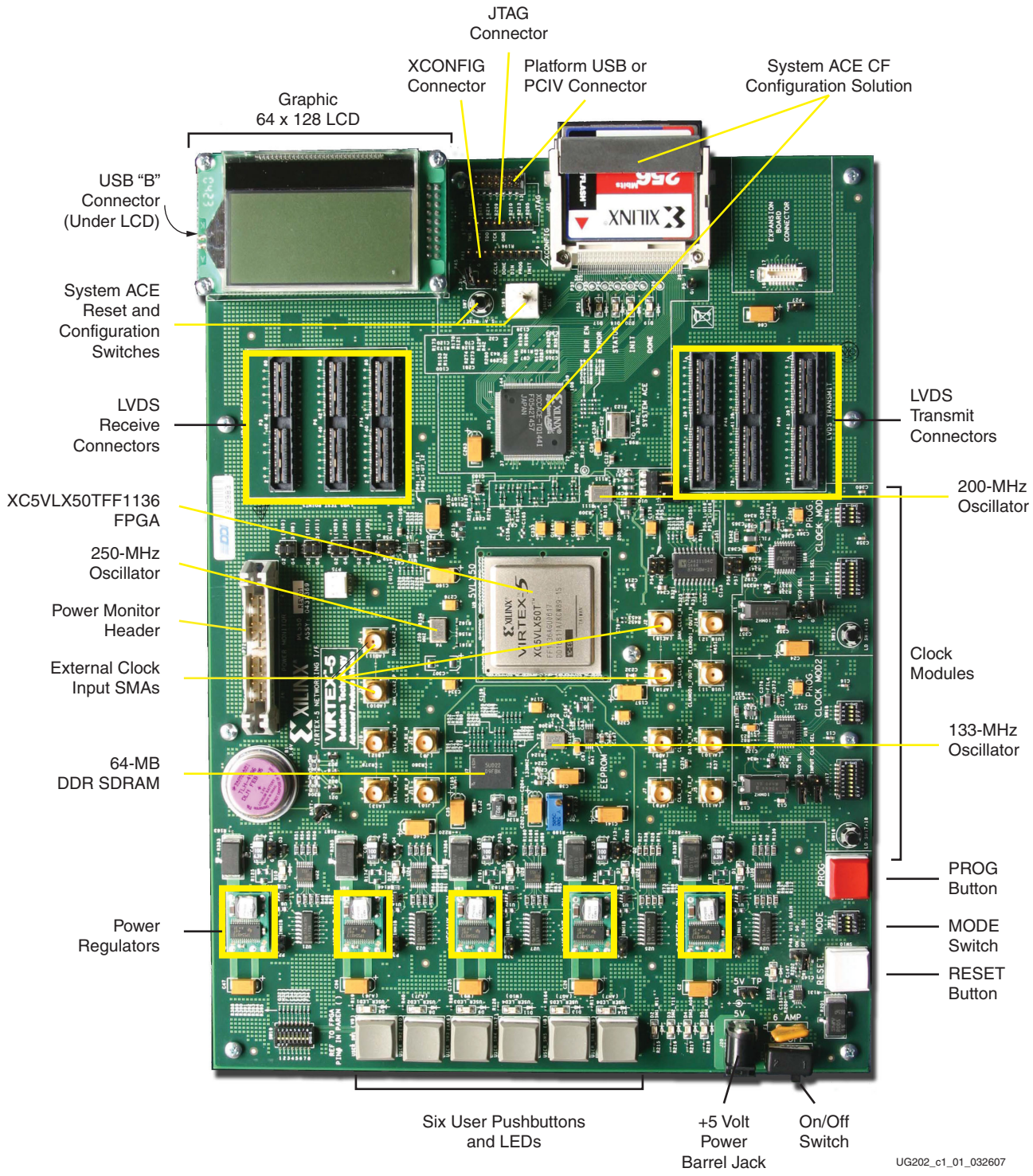

Figure 1-1: **Virtex-5 FPGA ML550 Networking Interfaces Development Board**

Chapter 2

Getting Started

This chapter describes the items needed to configure the Virtex-5 FPGA ML550 Networking Interfaces Development Board. The ML550 Development Board is tested at the factory after assembly and should be received in working condition. It is set up to load a bitstream from the CompactFlash card through the System ACE controller U13.

Documentation and Reference Design CD-ROM

The CD-ROM included in the Virtex-5 FPGA ML550 Source-Synchronous Interfaces Tool Kit contains the design files for the ML550 Networking Interfaces Platform, including schematics, board layout, and reference design files. Open the `ReadMe.txt` file on the CD-ROM to review the list of contents.

Quick Start Guide

Welcome to the ML550 Source Synchronous Interfaces Tool Kit!

Initial Setup

Check Kit Contents

The ML550 shipping carton contains:

- ML550 Board
- Compact Flash Card
- CD-ROM
- 120/240 VAC to 5 VDC 6A power supply with country-specific line cord
- USB Cable, B-to-A
- LVDS Loopback Board
- Welcome letter
- Misc. Xilinx Promo Kits and documentation

Unpack the Kit and Make Connections

- Remove the ML550 from the anti-static bag. Confirm that Power slide switch is OFF. Do not turn Power ON until instructed to do so.
- Remove the LVDS Loopback board from its bag, and install it on the ML550.
- Remove the Compact Flash card from its bag and install it into the ML550 at J21.

- Plug the 5V power supply line cord into a power outlet, and plug the barrel plug into the ML550 J20 jack.
- Plug the "B" end of the kit USB cable into the ML550 (the jack is under the LCD), and plug the "A" end into a PC USB port.

Installation

Silicon Labs USB-to-RS232 Bridge Chip Driver Installation

Assumptions:

- PC operating system is Microsoft Windows XP
- No previous versions of this driver have been installed on the PC
- The ML550 board is powered OFF
- The USB B-to-A cable is installed between the ML550 and the PC

1. Copy the ML550 BERT REV1.x.zip file from the kit CD-ROM to `C:\`.
2. Unzip the file. When this file is unzipped, a folder called `ML550 BERT REV1.x` is created.
3. Locate the self-extracting ZIP file `CP210x_Drivers.exe` in the folder `C:\ML550 BERT Rev1.x\USB_2_Serial Driver`. Double-click on this file.

   If the default target directory isn't changed, the folder `C:\SiLabs\MCU\CP210x` is created. This folder contains various drivers.
4. Turn on the ML550 power.

   Windows XP recognizes that new hardware is present, and opens the Add New Hardware Wizard.
5. Choose **Install from a list or specific location** and click **Next**.
6. Choose **Search for the best driver in these locations**. Enter the path `C:\SiLabs\MCU\CP210x\WIN` and click **Next**.
7. The wizard installs a driver and reports:

   ```
   The wizard has finished installing the software for CP2101 USB
   Composite Device.
   ```

   Click **Finish**.
8. Windows XP now recognizes the USB to Serial Bridge and wants to install its driver as well. Repeat step 5 and step 6.
9. The wizard installs another driver and reports:

   ```
   The wizard has finished installing the software for CP2101 USB to
   UART Bridge Controller.
   ```
10. Windows XP displays:

    ```
    Your new hardware is installed and ready to use.
    ```

Note: This driver assigns itself the lowest *unassigned* serial COM port number. This number varies with PC hardware configuration. COM3 or COM4 is typically assigned.

BERT GUI Tcl Interface Installation

1. Locate executable file `ActiveTcl8.4.7.0-win32-ix86-108887.exe` in `C:\ML550 BERT REV1.x` and double-click on it.
2. The Active State Active Tcl installer opens. Follow the dialog and accept the defaults.

   At the end of the process, the installer reports the folders created during the install. Click **Finish**.
3. Create a GUI shortcut for the Windows desktop:
   a. Locate executable file `gui_rev1.x.exe` in `C:\ML550 BERT REV1.x\GUI_Rev1.x`.
   b. Right-click on this file and choose **Create shortcut**.
   c. Drag the shortcut to the Windows XP desktop.

The BERT GUI is now ready to use.

ML550 Board Startup and Operation

1. Turn OFF the ML550 power.
2. Install either the LVDS Loopback board across the six LVDS Samtec connectors (if not already installed), or install a single Blue Ribbon cable between the center TX and RX Samtec connectors, P46 and P6 respectively.
3. Install the Compact Flash card into the J21 socket (if not already installed).
4. Confirm that the flash card image select rotary switch SW9 is set to position 0.
5. The CLOCK MOD 1 & 2 parallel programming DIP switches default to all OFF and can be safely ignored.

   The BERT test uses Clock Module 2 / U19. The GUI sets the Clock Module 2 / U19 initial frequency to 400 MHz.
6. Turn ON the ML550 power. The DONE LED D19 should come on.
7. On the PC, double-click on the `gui_rev1.x.exe` shortcut. The BERT GUI launches.
8. At the upper left are two selection boxes. The upper chooses the COM port, the lower chooses the test type. Click on the upper and select **COM4**. Click on the lower and select **PRBS15**.
9. Click on the big **Start/Restart** button.

   If the COM port is correct, the test begins.

   If the COM port is not correct, the GUI most likely will hang. If this occurs, close and relaunch the application. When repeating the selection sequence, choose COM3. If this also fails, repeat this procedure choosing a lower COM port number each time through.

   Some computers have more than four COM ports. It is possible that the USB-to-COM bridge driver will select a COM port that the GUI will not communicate with (e.g., COM14.) The workaround in this instance is to go to:

   Control Panel -> System -> Hardware -> Device Manager -> Ports

   Identify the port selected by the CP210x USB to UART driver. If the COM port is not **COM1**, **COM2**, **COM3**, or **COM4,** change the port using this path:

   Control Panel -> System -> Hardware -> Device Manager -> Ports -> CP210x USB to UART-> Port Settings -> Advanced COM Port Number

Select change to **COM#** where # is either 1, 2, 3, or 4.

10. The GUI reflects the frequency set at Clock Module 2 and initially reports 400 MHz. More information resides in the file `C:\ML550 BERT REV1.x\DDR_8TO1_16CHAN_PICO_REV1.x\README.doc`. Also refer to the `ML550 Networking Interfaces Board.ppt` presentation on the kit CD-ROM.
11. The clock frequency can be changed by clicking on the **+100 MHz**, **+10 MHz**, **–100 MHz**, and **–10 MHz** GUI buttons to the left of the Frequency display. More detailed information is available in the CD file `BERTGUI_README.doc`.

Programmable Clock Module Switch Position Chart

Four-Pole SW DIP2 Settings

	Switch Position			
	1	**2**	**3**	**4**
Always	OFF	OFF	OFF	OFF

Eight-Pole SW DIP1 Settings

	Switch Position							
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**
700 MHz	OFF	ON	ON	OFF	OFF	OFF	ON	OFF
690 MHz	ON	OFF	ON	OFF	OFF	OFF	ON	OFF
680 MHz	OFF	OFF	ON	OFF	OFF	OFF	ON	OFF
670 MHz	ON	ON	OFF	OFF	OFF	OFF	ON	OFF
660 MHz	OFF	ON	OFF	OFF	OFF	OFF	ON	OFF
650 MHz	ON	OFF	OFF	OFF	OFF	OFF	ON	OFF
600 MHz	OFF	OFF	ON	ON	ON	ON	OFF	OFF
400 MHz	OFF	OFF	OFF	ON	OFF	ON	OFF	OFF

Chapter 3

Hardware Description

A high-level block diagram of the Virtex-5 FPGA ML550 Networking Interfaces Development Board is shown in Figure 3-1, followed by a brief description of each board section.

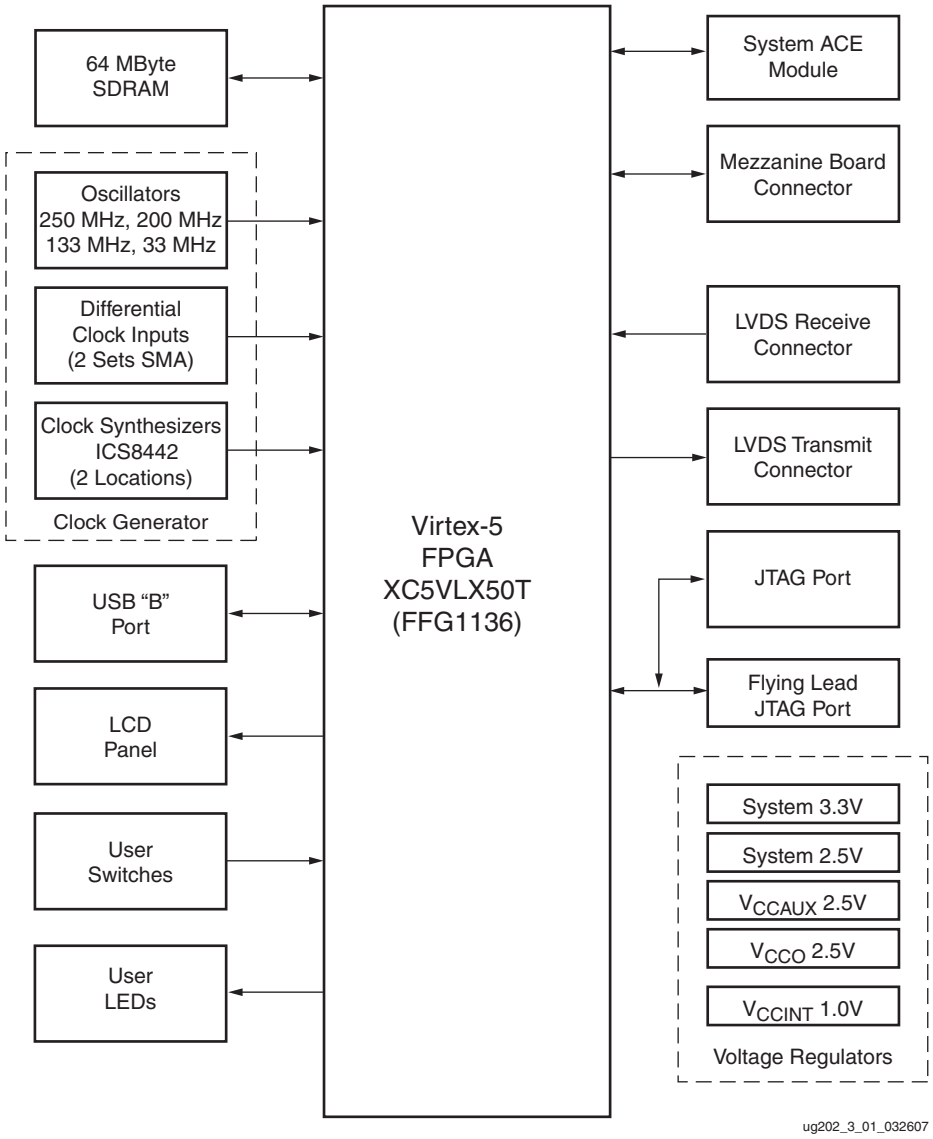

Figure 3-1: **Virtex-5 FPGA ML550 Networking Interfaces Development Board**

Clock Generation

The clock generation section of the ML550 Development Board provides all necessary clocks for the Virtex-5 FPGA. Eight clock sources are provided:

- Epson EG2121CA 2.5V 250-MHz differential LVPECL oscillator (Y4) for general use
- Epson EG2121CA 2.5V 200-MHz differential LVPECL oscillator (Y3) for Virtex-5 FPGA ISERDES support
- Epson EG2121CA 2.5V 133-MHz differential LVDS oscillator (Y2) for DDR memory interface
- Epson SG8002CA 3.3V 33-MHz LVCMOS single-ended oscillator (Y1) for SystemAce device (U13)
- Two differential SMA clock inputs (CLOCK-1: J3, J1 and CLOCK-2: J4, J2)
- Two clock synthesizer ICS8442 devices (U18,U19)

The differential SMA clock inputs are connected to the global clock inputs of the FPGA. An onboard 200-MHz oscillator calibrates the I/O delay, and an onboard 250-MHz oscillator is provided for general use.

The two ICS8442 clock synthesizer devices output differential LVDS clocks in the 31.25 MHz to 700 MHz range.

The on-chip LVDS differential terminator is recommended for use in designs. The clock is received by an IBUFGDS module, and beneath that module instantiation, the synthesis attribute DIFF_TERM must be set to TRUE. Refer to the *Virtex-5 FPGA User Guide* (UG190) for information and examples using SelectIO primitives for LVDS inputs.

Table 3-1 shows the clock generation components for the ML550 board.

Table 3-1: **Clock Generation – ML550 Rev 01 Board**

Clock Source Component	Reference Designator	Output Frequency	Output Type	Signal Name	FPGA Pin #		Bank
					P	N	
Epson SG8002CA	Y1	33 MHz	3.3V LVCMOS Single-Ended	SYSACE_CLK	V33	N/A	13
Epson EG2121CA	Y2	133 MHz	2.5V LVDS Differential	OSC_133M_P and N	R7	R8	12
Epson EG2121CA	Y3	200 MHz	2.5V LVPECL Differential	OSC_200M_P and N	L19	K19	3
Epson EG2121CA	Y4	250 MHz	2.5V LVPECL Differential	OSC_250M_P and N	H17	H18	3
ICS8442AY	U18	31.25 MHz	3.3V LVDS Differential #1	LVDSCLKMOD1_P and N	AH18	AG17	4
		to 700 MHz	3.3V LVDS Differential #2	CLKMOD1_FOUT1_P and N	J13	J14	N/A
ICS8442AY	U19	31.25 MHz	3.3V LVDS Differential #1	LVDSCLKMOD2A_P and N	AB30	AC30	17
		to 700 MHz	3.3V LVDS Differential #2	LVDSCLKMOD2B_P and N	AK28	AK27	21
SMA Connector	J1			SMA_CLK1_P	AF18	N/A	4
SMA Connector	J2			SMA_CLK1_N	N/A	AE18	4
SMA Connector	J3			SMA_CLK2_P	AD10	N/A	22
SMA Connector	J4			SMA_CLK2_N	N/A	AD11	22

SDRAM Memory

The ML550 Development Board provides 64 MBytes of SDRAM memory (Micron Semiconductor MT46V64M8BN-75). The high-level block diagram of the SDRAM interface is shown in Figure 3-2. Table 3-2 lists the SDRAM memory interface signals for the FFG1136 package used on the ML550 Development Board.

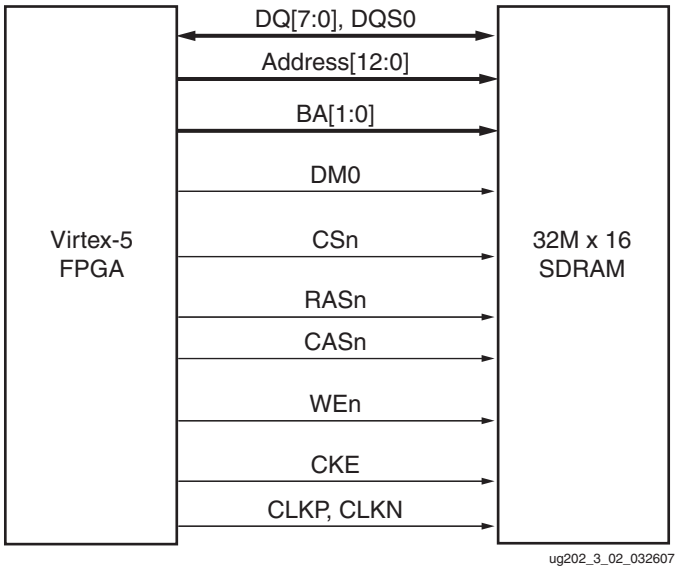

Figure 3-2: **Block Diagram of the SDRAM Interface**

Table 3-2: **SDRAM Memory Interface Signal Descriptions**

Signal Name	Description	FPGA Pin Number (FFG1136 Package, Bank 12)
A0	Address 0	J5
A1	Address 1	J6
A2	Address 2	T6
A3	Address 3	R6
A4	Address 4	K6
A5	Address 5	K7
A6	Address 6	P6
A7	Address 7	P7
A8	Address 8	L4
A9	Address 9	P5
A10	Address 10	N5
A11	Address 11	L6
A12	Address12	M7
DQ0	Data 0	T10
DQ1	Data 1	F6

Table 3-2: **SDRAM Memory Interface Signal Descriptions *(Continued)***

Signal Name	Description	FPGA Pin Number (FFG1136 Package, Bank 12)
DQ2	Data 2	F5
DQ3	Data 3	R11
DQ4	Data 4	N7
DQ5	Data 5	N8
DQ6	Data 6	M5
DQ7	Data 7	M6
DQS0(1)	DQ Strobe	T9
BA0	Bank Select 0	G6
BA1	Bank Select 1	T11
DM0	Write Mask	G7
CSn	Chip Select	E7
RASn	Row Address Strobe	U7
CASn	Column Address Strobe	T8
WEn	Write Enable	E6
CLK_P	Positive Clock	H7
CLK_N	Negative Clock	J7
CKE	Clock Enable	U10

Notes:

1. Because DQS0 is not located on a clock capable I/O pin, the Xilinx MIG tool cannot be used to generate a SDRAM memory controller for the 64M x 8 SDRAM on the ML550 board.

Liquid Crystal Display

The ML550 Development Board provides an 8-bit interface to a 64 x 128 LCD panel (DisplayTechQ 64128E-FC-BC-3LP, 64 x 128). This display was chosen because of its possible use in embedded systems. Appendix C, "LCD Interface," describes the LCD operation in detail.

Table 3-3 describes the LCD interface signal descriptions for the FFG1136 package used on the ML550 Development Board.

Table 3-3: **LCD Interface Signal Descriptions**

Signal Name	LCD Pin Number	Description	FPGA Pin Number (FFG1136 Package, Bank 13)
V_{SS}	1	GND	Ground
V_{DD}	2	3.3V DC	Logic Supply
MI	3	H = 6800 CPU, L = 8080 CPU	Pull-up R14 to 3.3V
DB7	4	LCD Data Bit 7	AK33

Table 3-3: **LCD Interface Signal Descriptions *(Continued)***

Signal Name	LCD Pin Number	Description	FPGA Pin Number (FFG1136 Package, Bank 13)
DB6	5	LCD Data Bit 6	AG32
DB5	6	LCD Data Bit 5	AH32
DB4	7	LCD Data Bit 4	AJ32
DB3	8	LCD Data Bit 3	AK32
DB2	9	LCD Data Bit 2	AL34
DB1	10	LCD Data Bit 1	AL33
DB0	11	LCD Data Bit 0	AM33
E	12	LCD Enable	AN33
R/W	13	LCD Write	AN32
RS	14	LCD Register Select	AP32
RST	15	LCD Reset	AM32
CS1B	16	LCD Chip Select	AN34
LED +	17	LCD Backlight Anode	Ctrl. Transistor Q1
LED –	18	LCD Backlight Cathode	Ground
LCD_BL_ON	N/A	LCD Backlight Control	AK34

The LCD can display alphanumeric (ASCII) information; however, a hardware character generator must be designed in the FPGA fabric in order to display the characters on the LCD screen. A character-type display (with on-board character generator) can also be connected because the graphical LCD has the same interface as many character-type LCD panels.

Display Hardware Design

The I/Os of the FPGA function at 2.5V. The FPGA is connected to the graphic LCD display through a set of voltage-level converting devices. These switches translate the 2.5V I/O signals to the 3.3V signals that the LCD display requires.

Control for the LCD panel is based on the KS0713 controller from Samsung. The KS0713 is a 65-column, 132-segment driver-controller device for graphic dot matrix LCD display systems. The chip accepts serial or parallel display data. The 8-bit parallel interface is compatible with most LCD panel manufacturers. The serial connection mode is write only.

Extra features added to the interface in addition to the normal parallel signals are:

- Intel or Motorola compatible interface
- External reset of the chip
- External chip select

The interface also contains the following built-in options for the display and controller:

- On-chip oscillator circuitry
- On-chip voltage converter (x2, x3, x4, and x5)

- A 64-step electronic contrast control function

Table 3-4 summarizes the controller specifications.

Table 3-4: **Display Controller Specifications**

Parameter	Specification
Supply Voltage	2.4V to 3.6V (V_{DD})
LCD Driving Voltage	4V to 15V ($V_{LCD} = V_0 - V_{DD}$) Generated On-Chip
Power Consumption	70 µA typical (V_{DD} = 3V, x4 boost, V_0 = 11V, internal supply = ON)
Sleep Mode	2 µA
Standby Mode	10 µA

Hardware Schematic Diagrams

Figure 3-3 shows the schematic for connections to the display. Figure 3-4 shows a block diagram of the display, and Figure 3-5 shows the dimensions of the display.

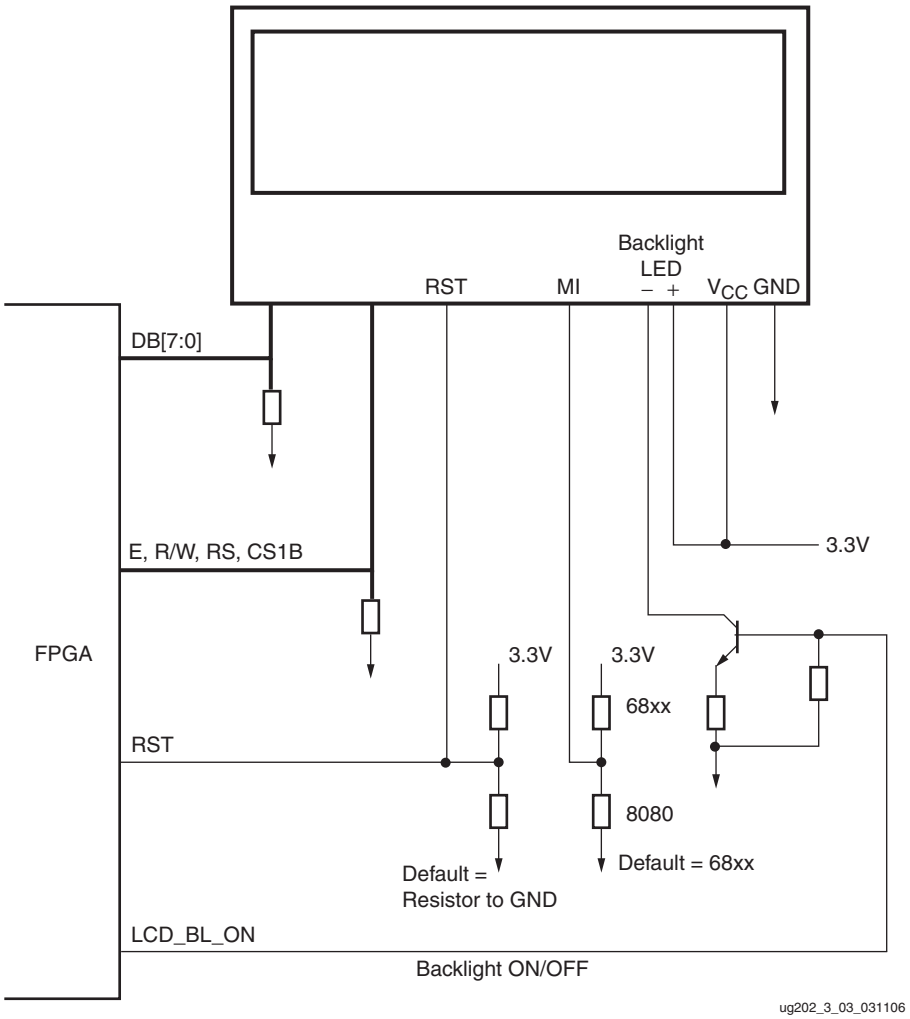

Figure 3-3: **Display Schematic Diagram**

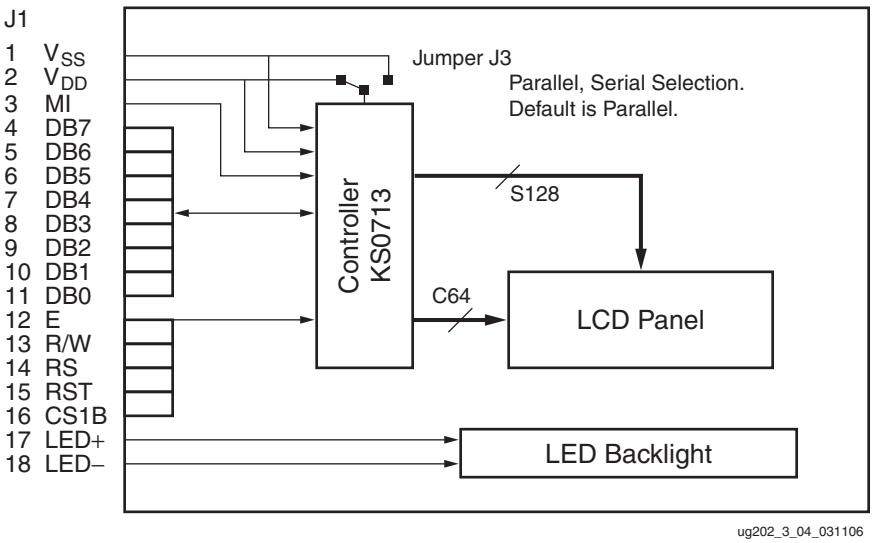

Figure 3-4: **64128EFCBC-3LP Block Diagram**

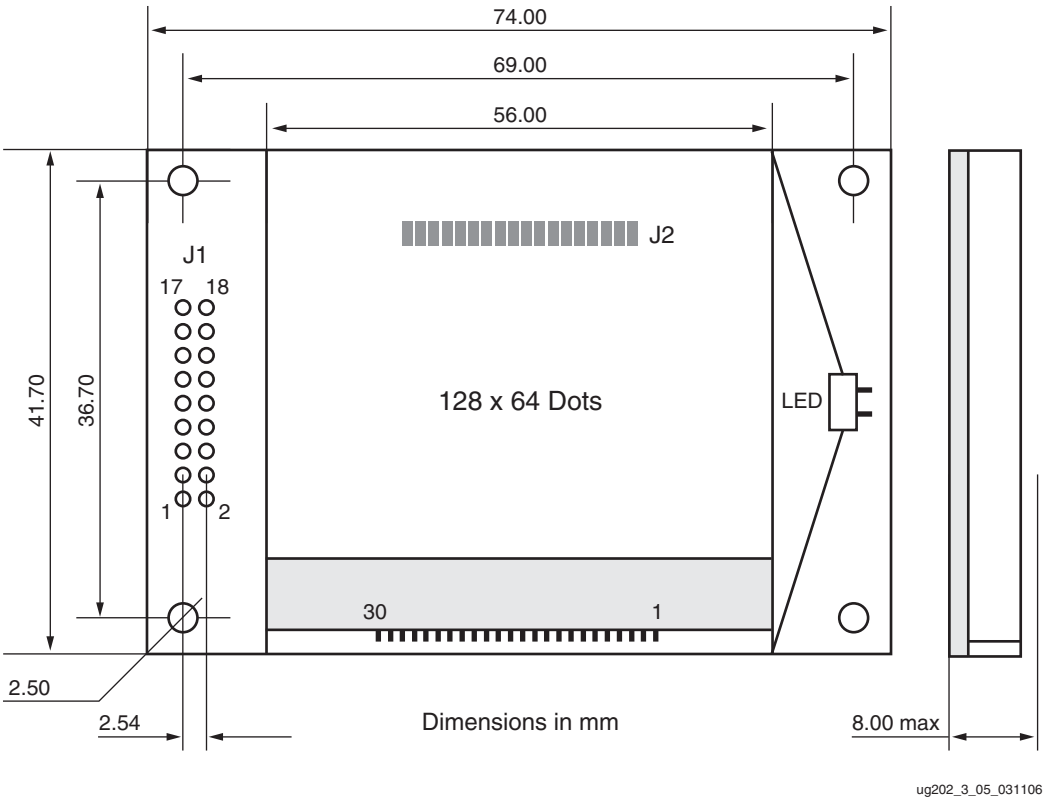

Figure 3-5: **64128EFCBC-3LP Dimensions**

User LED

The ML550 Development Board provides six user LEDs that can be turned ON by driving the LEDs signal Low. Table 3-5 describes the user LEDs and their associated pin assignments for the FFG1136 FPGA used on the ML550 Development Board.

Table 3-5: **User LED Pin Assignments**

LED	Designation	FPGA Pin Number (FFG1136 Package, Bank 18)
USER_LED1	USER_LED1 D6	AJ6
USER_LED2	USER_LED2 D8	AJ7
USER_LED3	USER_LED3 D9	W9
USER_LED4	USER_LED4 D11	W10
USER_LED5	USER_LED5 D13	AG7
USER_LED6	USER_LED6 D14	AH7

Configuration INIT and DONE LEDs

The ML550 Development Board provides an INIT LED and a DONE LED, which are activated by drive transistors responding to the INIT_B (N14) and DONE (M15) FPGA signals respectively. Table 3-6 describes these LEDs and their associated pin assignments for the FFG1136 FPGA used on the ML550 Development Board.

Table 3-6: **Configuration INIT and DONE LED Pin Assignments**

LED	Designation	FPGA Pin Number (FFG1136 Package)
FPGA_INIT_B	INIT D20	N14
FPGA_DONE	DONE D19	M15

User Push-Button Switches

The ML550 Development Board provides six user push-button switches that generate an active-Low signal when a given switch is pressed (see Table 3-7). There are pull-up resistors on the push-button switch signals on the ML550 Development Board. The internal FPGA pull-up resistors do not need to be used to force a given push-button switch signal High when its associated switch is not pressed. Switch contact debounce logic must be implemented inside the FPGA.

Table 3-7: **User Push-Button Switch Assignments**

Signal Switch Designation	Description	FPGA Pin Number (FFG1136 Package, Bank 18)
USER_SW1	USER_SW1	V9
USER_SW2	USER_SW2	V10
USER_SW3	USER_SW3	AK6
USER_ SW4	USER_ SW4	AK7
USER_SW5	USER_SW5	U8
USER_SW6	USER_SW6	V8
FPGA_RESETB SW10	RESET	W34, Bank 13

Program Switch

The ML550 Development Board provides a push-button program switch (SW12) for initiating the configuration of the Virtex-5 FPGA. This switch is used to force a reconfiguration of the FPGA from PROMs if they are present and enabled. The ML550 Development Board does not include PROMs.

The primary configuration device is the System ACE Controller (U13), which loads image files from a CompactFlash card. The mode DIP switch (SW11) must be set to the proper mode for configuration to occur via the System ACE interface (refer to "Configuration Modes" on page 45 for further information regarding setting mode jumpers). The PROG push button simply clears the FPGA configuration on this board.

USB Port (J22)

The ML550 development board provides a USB "B" connector for interface to a PC (using a USB B-to-A cable.) The board uses a Silicon Labs 3.3V CP2102 USB-to-RS232 converter device (U2) to drive the RD, TD, RTS, and CTS signals to the FPGA via a Maxim MAX3008 level translator (U20). The user must provide a UART core internal to the FPGA to enable serial communication. A Silicon Labs CP2102 driver file is included on the ML550 development kit CD. This driver allows a PC USB port to be configured as a serial COM port for the user to continue working with serial communication utilities like HyperTerminal or Tera Term Pro.

Table 3-8 describes the USB interface signal names and their respective Virtex-5 FPGA pin assignments.

Table 3-8: **RS-232 Interface Signal Names and Pin Assignments**

USB J22 Pin #	USB Signal	CP2102 USB I/F U2 Pin #	CP2102 RS232 I/F U2 Pin #	CP2102 RS232 Signal	U20 USB-Side Pin #	U20 FPGA-Side Pin #	U20 to FPGA 2.5V I/O Signal Name	FPGA U9 Bank 11 Pin #
1	USB_VBUS	8	28	USB_DTR_I_B	7	14	USB_DTR_B	C33
2	USB_D-	5	27	USB_DSR_I_B	3	18	USB_DSR_B	D34
3	USB_D+	4	26	USB_TX_O	8	13	USB_TX	B33
4	GND	3	25	USB_RX_I	4	17	USB_RX	C34
			24	USB_RTS_O_B	9	12	USB_RTS_B	A33
			23	USB_CTS_I_B	5	16	USB_CTS_B	D32
			9	USB_RESET_I_B	1	20	USB_RESET_B	B32
			12	USB_SUSPEND_O	6	15	USB_SUSPEND	C32

A high-level block diagram of the USB interface is shown in Figure 3-6. The USB B-to-A cable included in the kit mates with the J22 connector.

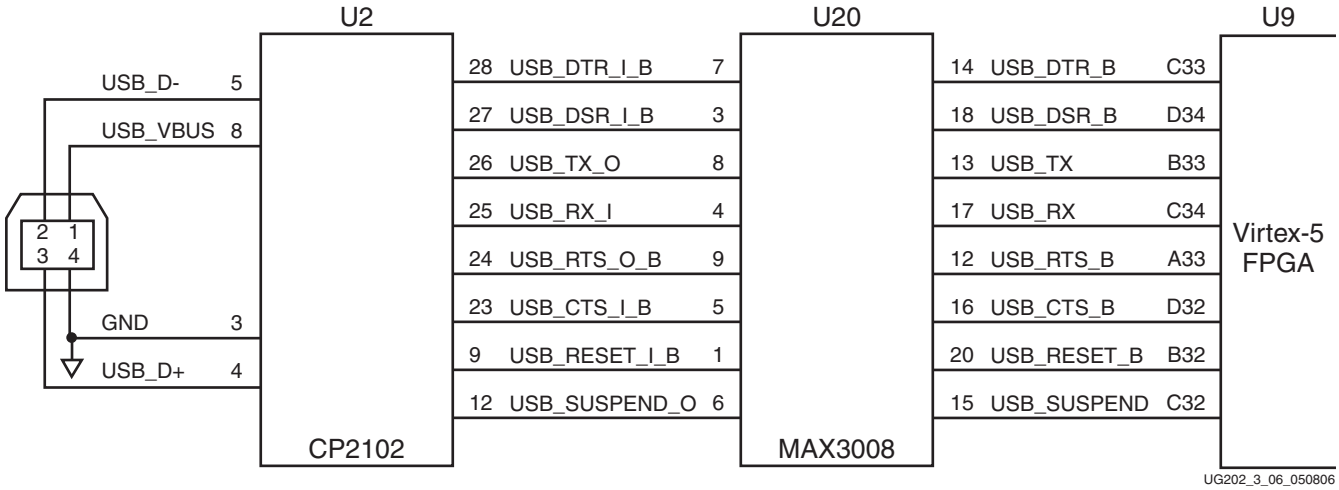

Figure 3-6: **USB Interface Block Diagram**

LVDS Connectors

The ML550 Development Board provides 53 pairs of transmit signals and 53 pairs of receive LVDS signals. These signals are distributed across three Samtec QSE-DP connectors for transmitting and another three connectors for receiving. Appendix A, "LVDS," lists the pinouts.

Transmit LVDS

The LVDS transmit connectors are shown on schematic pages 6 (TX1, P73, U9 bank 17), 7 (TX2, P46, U9 bank 21) and 8 (TX3, P49, U9 bank 22).

ML550 schematic 0381218 sheet 7 shows FPGA U9.AJ26/AJ25 FPGA_CLKP/N from the FPGA driving a clock multiplier device U16 detailed on sheet 12. On sheet 12, the U16 ICS8745B clock multiplier is configured in clock-doubler mode. U16 receives the FPGA_CLKP/N clock waveform on it's input pins U16.1 and U16.2, and outputs a doubled frequency on pins U16.13 and U16.12, XMITCLK_P and XMITCLK_N respectively. This doubled output clock is wired to a Samtec LVDS transmit connector P46, pins P46.40 and P46.38, on sheet 7.

Receive LVDS

The LVDS receive connectors are shown on schematic pages 9 (RX1, P74, U9 bank 15), 10 (RX2, P6, U9 bank 19) and 11 (RX3, P3, U9 bank 20).

Each FPGA U9 bank V_{CCO} is 2.5V, and the intended signalling standard for the LVDS interface is LVDS_25.

ML550 schematic 0381218 sheet 10 shows FPGA U9.E28/F28 DIVCLKP/N driven from a clock divider device U17 detailed on sheet 12. On sheet 12, the U17 On Semi NB6N239S clock divider is configured in divide-by-2 mode. U17 receives the clock waveform from the Samtec LVDS receive connector P6 pins P6.47 and P6.49, on sheet 10. This RCVCLK_P and RCVCLK_N clock waveform drives U17 input pins U17.2 and U17.3 respectively. U17 then

outputs a halved frequency on pins U17.12 and U17.11, DIVCLK_P and DIVCLK_N respectively. As previously mentioned, these output pins are connected to the FPGA.

LVDS Loopback Board (Xilinx P/N 0431395)

LVDS transmit to receive loopback can be achieved with either the LVDS Loopback board included in the kit, or with the Precision Interconnect Blue Ribbon Cables (Xilinx P/N HW-LVDS-CBL-80, order separately). Appendix B, "LVDS Loopback Board" includes LVDS Loopback Board details.

Voltage Regulators (TI PTH05000)

Figure 3-7 shows the voltage regulators used on ML550 Development Board to provide various on-board voltage sources. As shown in Figure 3-7, connector J20 provides the main 5.0V voltage to the board. This voltage source is provided to all on-board regulators to generate the 1.0V, 2.5V, and 3.3V voltages for the digital section of the board. All Bank V_{CCO} voltages are 2.5V.

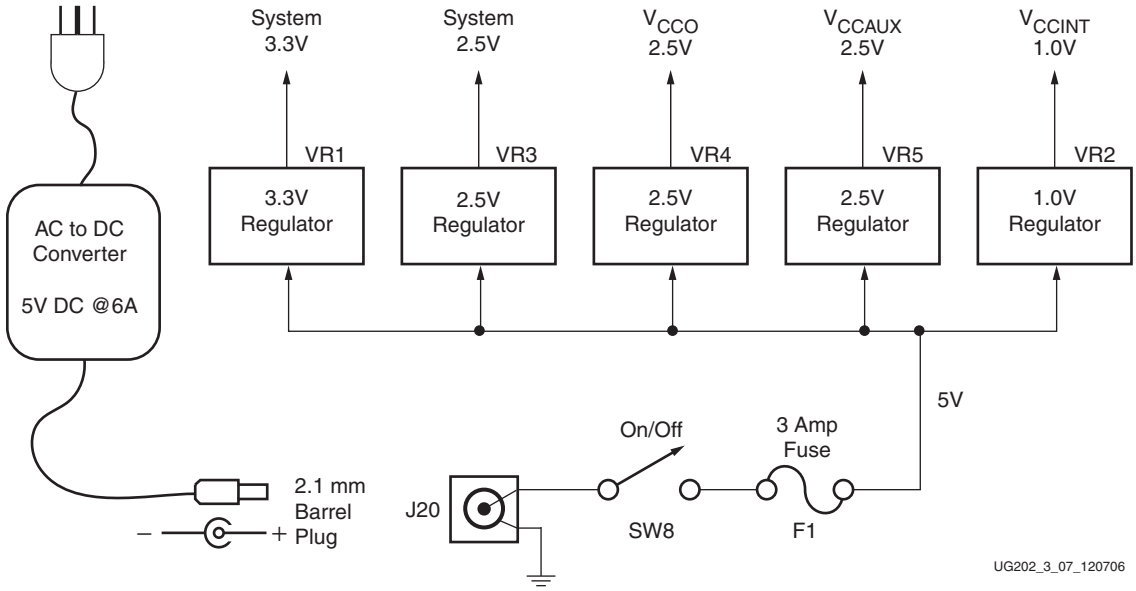

Figure 3-7: **Block Diagram of the Five Voltage Regulators**

Onboard digital voltages are as follows:

- 1.0V V_{CCINT} (VR2)
- 2.5V V_{CCAUX} (VR5)
- 2.5V V_{CCO} (VR4)
- 2.5V System (VR3)
- 3.3V System (VR1)

Voltage Regulator ±5% Margin Adjustment (in 2.5% Increments)

The regulators shown in Table 3-9 can have their outputs controlled over a ±5% range by the FPGA, or they can be enabled or inhibited through the use of on-board jumpers. The jumpers use the following conventions:

- Jumper OFF = Enabled
- Jumper ON = Inhibited

The TI PTH05000 regulator module requires a fixed 5V input. The output is adjustable over a range of 0.9V to 3.6V by changing the resistor tied between pin 4 and GND.

Table 3-9: **Voltage Regulators VR1 through VR5**

Regulator	Inhibit Jumper	Test Point Connector	Margin Control Strobes	V_{OUT} Target Voltage (V)(1)								
				–10%	–7.5%	–5%	–2.5%	Nom	+2.5%	+5%	+7.5%	+10%
VR1 System 3.3V	P4	P1	STB_SYS3V3 (FPGA U9:AD4)	2.97	3.05	3.14	3.22	3.30	3.383	3.465	3.548	3.63
VR2 V_{CCINT} 1.0V	P14	P13	STB_VCCINT1V0 (FPGA U9:AA6)	0.90	0.93	0.95	0.98	1.00	1.025	1.05	1.075	1.1
VR3 System 2.5V	P21	P16	STB_SYS2V5 (FPGA U9:AD6)	2.25	2.31	2.38	2.44	2.50	2.563	2.625	2.688	2.75
VR4 V_{CCO} 2.5V	P30	P22	STB_VCCO2V5 (FPGA U9:Y7)	2.25	2.31	2.38	2.44	2.50	2.563	2.625	2.688	2.75
VR5 V_{CCAUX} 2.5V	P38	P33	STB_VCCAUX2V5 (FPGA U9:AD5)	2.25	2.31	2.38	2.44	2.50	2.563	2.625	2.688	2.75

Notes:

1. ±5% margin limit.

Table 3-10 shows the VR_SEL[3:0] settings used to control the voltage regulator outputs. Table 3-11 lists the pin locations for VR_SEL[3:0].

Table 3-10: **Voltage Regulator Output Select VR_SEL**

VR_SEL[3:0]				V_{OUT} Selected(1)
3	2	1	0	
0	0	0	1	–10%
0	0	1	1	–7.5%
0	1	0	1	–5%
0	1	1	1	–2.5%
-	-	-	0	Nominal
1	0	0	1	+2.5%
1	0	1	1	+5%
1	1	0	1	+7.5%
1	1	1	1	+10%

Notes:

1. ±5% margin limit.
2. At power-on, FPGA_RESETB (FPGA U9.W34) is not driven and is pulled down by a 4.7 KΩ resistor.
3. At power-on, V_{REG} defaults to the nominal output.
4. To enable margin control, the U9.W34 FPGA_RESETB pin must be driven High.
5. To select other than the nominal output, set up the margin % on VR_SEL[3:0], then strobe the appropriate STB_* from Low to High to Low to clock the value into the latch.

Table 3-11: **VR_SEL[3:0] FPGA Pinout**

VR_SEL[3:0] Signal	FPGA Pin #
VR_SEL0	AE7
VR_SEL1	Y6
VR_SEL2	W6
VR_SEL3	AE6

The ML550 Networking Interfaces Platform implements the remote ±5% output adjustment using two Maxim analog mux devices: an 8-to-1 for the margin R_{ADJ} selection and a 2-to-1 to select between the output of the 8-to-1 mux or the R_{NOM} resistor that sets the voltage regulator output to its nominal value. These analog muxes have analog switch resistance on the order of 1Ω. Each voltage regulator has its own independent margin control capabilities as shown in Figure 3-8 and Figure 3-9. Figure 3-8 shows a typical schematic for voltage regulator control.

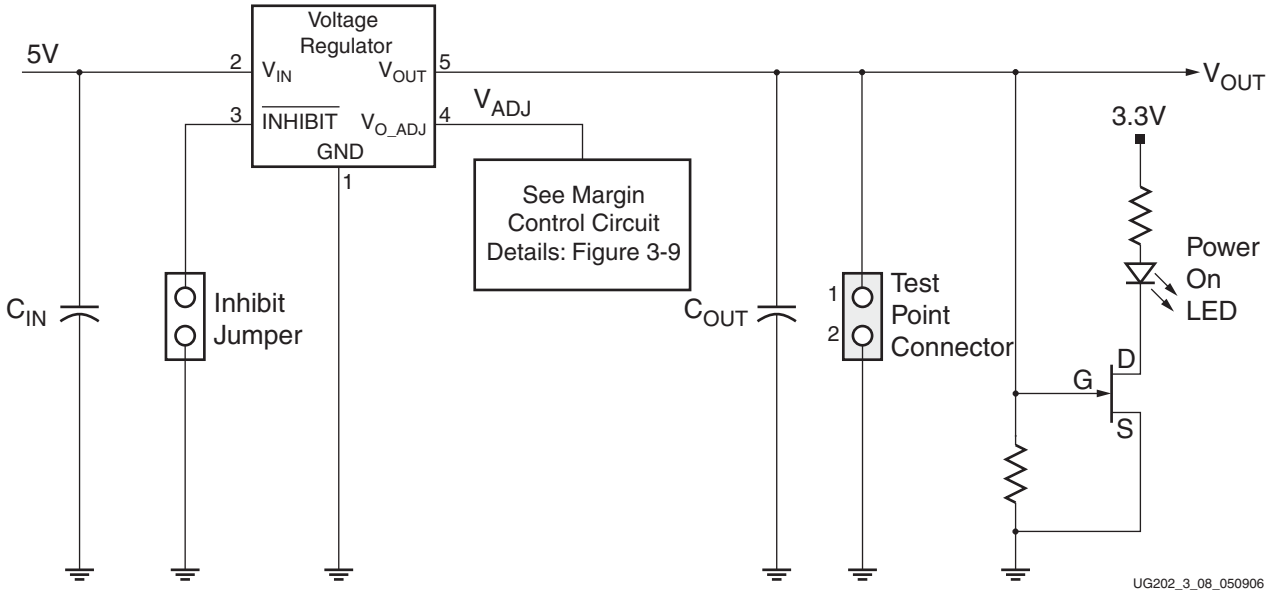

Figure 3-8: **Typical Voltage Regulator Configuration**

Important Note About ± 5% Margin Limits

Xilinx devices are specified to work over ±5% power rail variations. In Figure 3-9, the two outer margin resistors in the ±10% and ±7.5% locations are set to the value which gives ±5% regulator output. Any changes to these resistor values that allow the regulator output to exceed ±5% will void the board warranty.

Figure 3-9 shows typical margin control circuit details.

Each regulator has similar margin control circuitry, only the Radj resistors vary between regulators. A pull-down resistor is tied to the FPGA_RESETB signal so that the default "nominal" regulator output value is selected at board power-up (before the FPGA has been configured). The normally closed switch in the 2-to-1 mux selects the "nominal" output adjustment resistor (R_{NOM}).

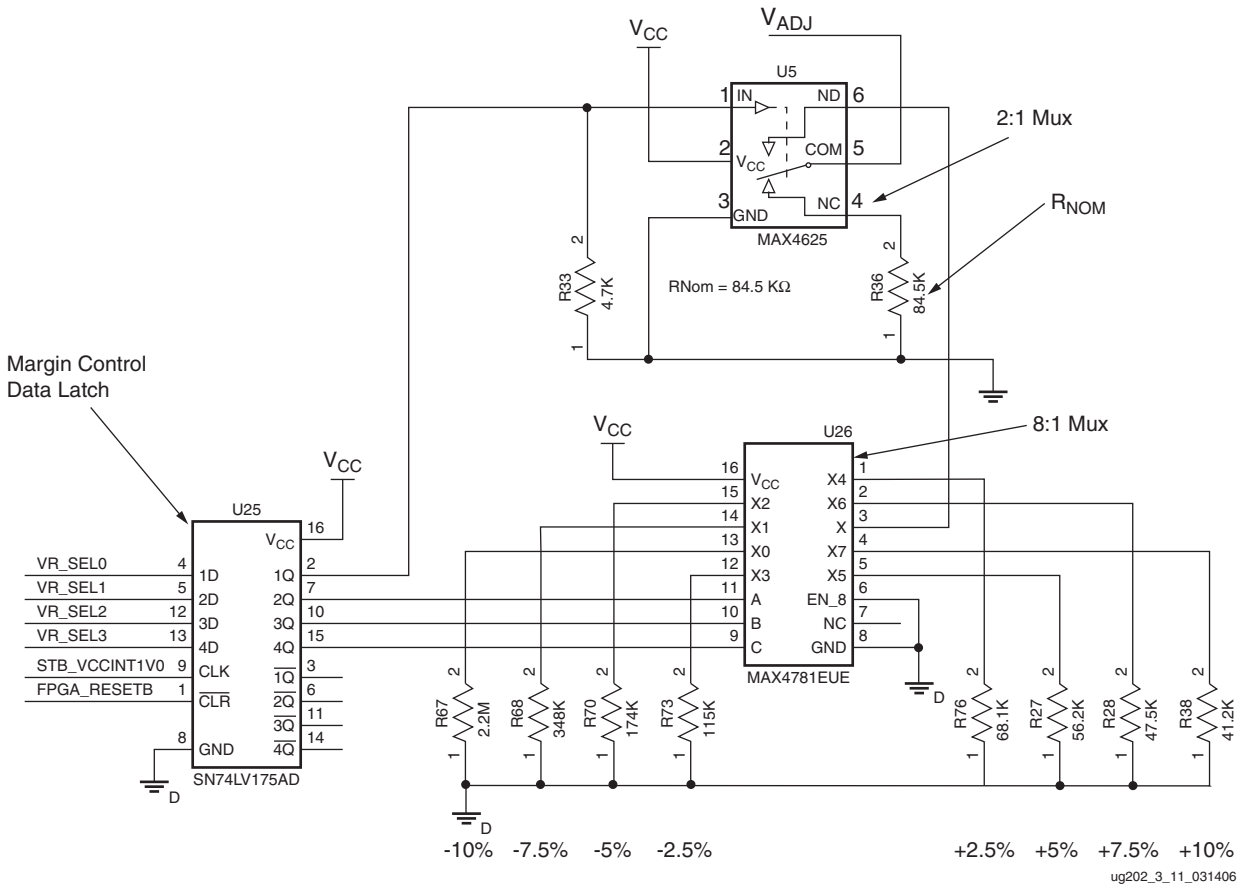

Figure 3-9: **Margin Control Circuit Details**

To activate the margin control circuitry FPGA_RESETB is driven High, the desired margin resistor select data is setup on the VR_SEL[3:0] bus, and the data latch of the voltage regulator of interest is strobed to capture the resistor select data. See Margin Control Strobes in Table 3-9. The latch output drives the analog mux switch select lines to cause selection of the appropriate R_{ADJ} resistor, which causes the regulator to adjust its output to the selected margin voltage value.

Each regulator has a two-pin test point connector associated with it (pin 1 = V_{OUT} and pin 2 = GND). To apply V_{OUT} values other than the fixed set the voltage regulator can supply, first disable the on-board voltage regulator using the inhibit jumper shown in Figure 3-8, and then connect a bench-top power supply to the two-pin test point connector for that voltage. This provides bench-top power to the power plane and also "back powers" the output pin of the inhibited voltage regulator.

Note: Do not turn OFF the 5V power to the ML550 Development Board while a bench-top power supply is ON and attached to the board in the manner described above. The voltage regulator can be damaged if the output is reverse powered and the 5V input is removed. Always turn the bench-top power supply OFF first, then turn the 5V power to the ML550 Development Board OFF.

Power Monitor Connector

Not shown in Figure 3-8 or Figure 3-9 is the voltage plane current measurement resistor. Each voltage regulator is routed to its own 10 mΩ1% 3W Kelvin current sense resistor. The

voltage taps on each resistor are wired to the P72 Power Monitor connector. Figure 3-10 shows a typical current sense resistor topology.

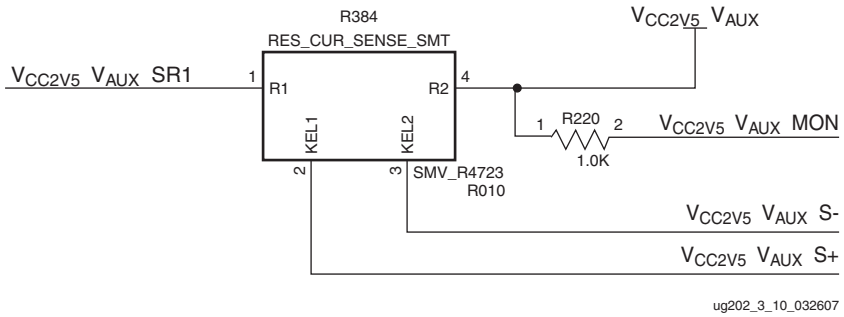

Figure 3-10: **Typical Current Sense Resistor Topology**

In this case, $V_{CC2V5\_VAUX\_SR1}$ is the 2.5V V_{AUX} voltage regulator output trace. It is connected to the "input" side of a 10 mΩ1% Kelvin resistor. The "output" side of the resistor feeds the 2.5V V_{AUX} power plane.

Each ML550 voltage regulator output is connected to P72 to permit power plane current measurements, which can in turn be used in power consumption calculations, recalling that Power (P) = Voltage (V) x Current (I), and that in the case of the current sense resistor, Current (I) = Sensed Voltage (V_S)/0.010Ω The resulting power measurement equation is:

$$P = V \times (V_S/0.010) \text{ Watts}$$

The ML550 +5V input is also connected through a current measurement resistor. The value of the resistor (R201) is 5 mΩ When measuring current using the +5V signals at P72, V_{CC5_S+} and V_{CC5_S-}, the power measurement equation is modified to:

$$P = V \times (V_S/0.005) \text{ Watts}$$

Table 3-12 shows the power measurement header P72 connections of the voltage regulator sense resistors. Refer to Figure 3-21, page 42 and Table 3-16, page 43 for complete P72 pinout details.

Table 3-12: **Power Measurement P72 Pinout**

Power Plane	Regulator	Nominal V_{OUT}	P72 Pin Number			R_{SENSE}	R (mΩ)
			S+	S–	MON		
V_{CC5}(1)	J20	5.18V input	25	26	24	R201	5
V_{CC3V3}	VR1	3.30V	17	18	19	R387	10
V_{CC1V0}	VR2	1.00V	1	2	3	R386	10
V_{CC2V5_VCCO}	VR4	2.50V	9	10	11	R385	10
V_{CC2V5}	VR3	2.50V	13	14	15	R383	10
V_{CC2V5_VAUX}	VR5	2.50V	5	6	7	R384	10

Notes:

1. V_{CC5} power available on P72 pin 20.
2. P72 GND pins: 4, 8, 12, 16.
3. ML550 errata: Due to a layout component library error, the S+ and S– pin connections are reversed. To obtain a positive DVM reading, apply the negative lead to the S+ pin, and the positive lead to the S– pin.
4. P72 is a 2 x 13 pin header (male) with pins on 0.1-inch centers.

ML550 System Monitor and Power Monitor Support

The Virtex-5 FPGA System Monitor block diagram is shown in Figure 3-11.

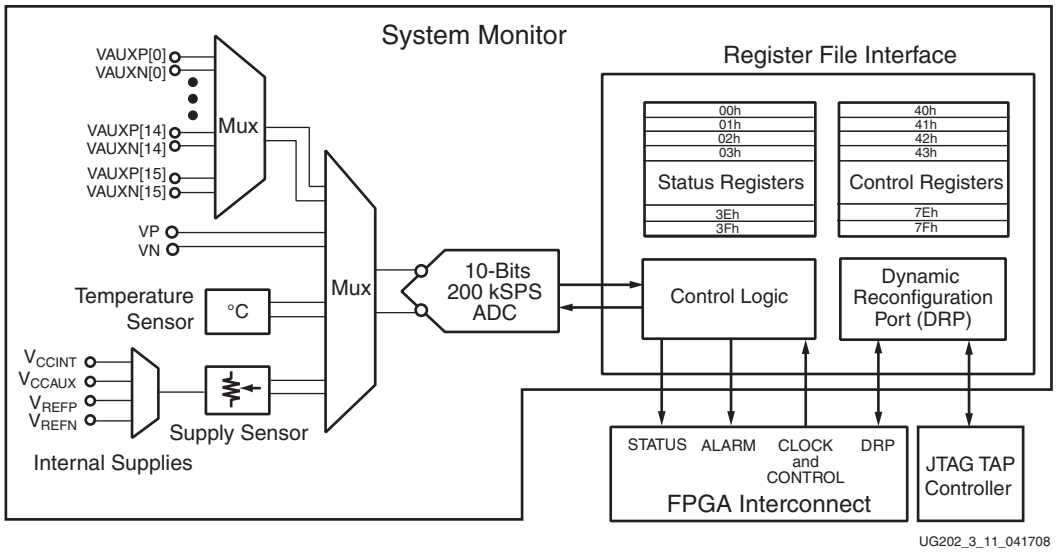

Figure 3-11: **Virtex-5 FPGA System Monitor**

The ML550 board hosts several measurement circuits, external to the FPGA, which are connected to the upper half of the input channels shown in the block diagram, namely the inputs VAUXP/N[9:15] and VP/VN). VAUXP/N[0:8] are not supported on the ML550 as these dual-purpose FPGA pins are used for other functions.

Detailed information concerning the System Monitor block is contained in UG192, available at the following link:

http://www.xilinx.com/support/documentation/user_guides/ug192.pdf

The ML550 system monitor support circuitry is connected to the XC5VLX50T FFG-1136 as shown in Table 3-13.

Table 3-13: **ML550 System Monitor Connections**

System Monitor Input Channel	FPGA Pin#	Parameter Measured	Signal Name	Sensor Circuit	Schematic Sheet(s)
VAUXN[9]	U31	5V Power (N)	VCC5V_MON_SM9N	R network	19, 34
VAUXP[9]	U32	5V Power (P)	VCC5V_MON_SM9P	R network	19, 34
VAUXN[10]	T34	2.5V V_{CCAUX} (N)	VCCAUX2V5_MON_SM10N	R network	20, 34
VAUXP[10]	U33	2.5V V_{CCAUX} (P)	VCCAUX2V5_MON_SM10P	R network	20, 34
VAUXN[11]	R32	2.5V V_{CCO} (N)	VCCO2V5_MON_SM11N	R network	20, 34
VAUXP[11]	R33	2.5V V_{CCO} (P)	VCCO2V5_MON_SM11P	R network	20, 34
VAUXN[12]	R34	2.5V System (N)	VCC2V5_MON_SM12N	R network	20, 34
VAUXP[12]	T33	2.5V System (P)	VCC2V5_MON_SM12P	R network	20, 34
VAUXN[13]	N32	1.0V V_{CCINT} (N)	VCC1V0_MON_SM13N	R network	20, 34
VAUXP[13]	P32	1.0V V_{CCINT} (P)	VCC1V0_MON_SM13P	R network	20, 34

Table 3-13: **ML550 System Monitor Connections *(Continued)***

System Monitor Input Channel	FPGA Pin#	Parameter Measured	Signal Name	Sensor Circuit	Schematic Sheet(s)
VAUXN[14]	K32	5V Current (N)	VCC5_I_MEAS_SM14N	U15(1) + R network	19, 34
VAUXP[14]	K33	5V Current (P)	VCC5_I_MEAS_SM14P	U15(1) + R network	19, 34
VAUXN[15]	K34	PCB Temperature (N)	TEMP_MON_SM15N	U11(2) + R network	19, 34
VAUXP[15]	L34	PCB Temperature (P)	TEMP_MON_SM15P	U11(2) + R network	19, 34
VN	V17	J19.3 connector pin(3)	VN_SM	none	30
VP	U18	J19.1 connector pin(3)	VP_SM	none	30
n/a	N34	n/a	SM_GPIO1	none	30, 34
n/a	P34	n/a	SM_GPIO2	none	30, 34
n/a	M32	n/a	SM_GPIO3	none	30, 34
n/a	L33	n/a	SM_GPIO4	none	30, 34

Notes:

1. U15 = MAX4071 current sense amplifier
2. U11 = MAX6608 analog temperature sensor
3. J19 = Hirose expansion connector

ML550 Board System Monitor Support Circuitry Details

Figure 3-12 through Figure 3-21 use the following format to show to which schematic, device, and pin number the indicated signal connects:

S#,Des.P#

where:

- *S#* is the schematic sheet number (for example, 19)
- *Des* is the device reference designator (for example, U20)
- *P#* is the device pin number (for example, V18)

5V Input Power Voltage Monitor

The signal conditioning network is shown in Figure 3-12.

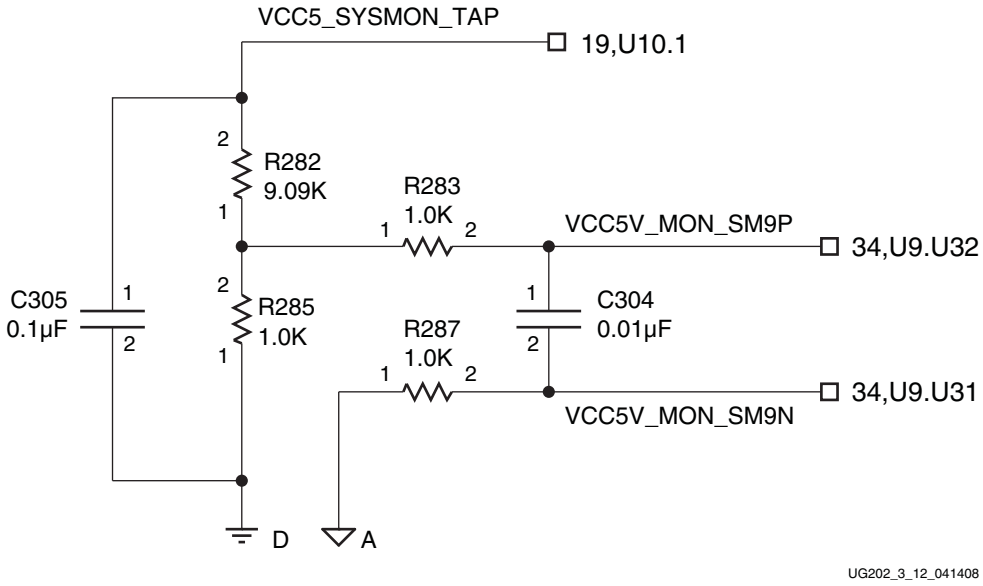

Figure 3-12: **5V Input Power Voltage Monitor (Sheet 19)**

2.5V V_{CCAUX} Voltage Monitor

The signal conditioning network is shown in Figure 3-13.

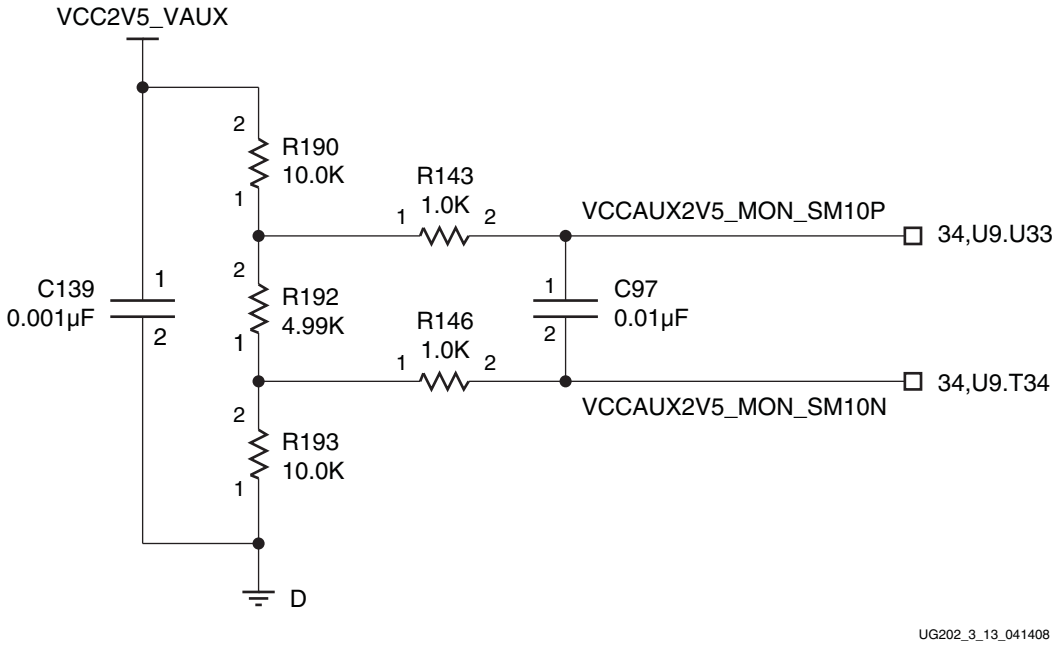

Figure 3-13: **2.5V V_{CCAUX} Voltage Monitor (Sheet 20)**

2.5V V_{CCO} Voltage Monitor

The signal conditioning network is shown in Figure 3-14.

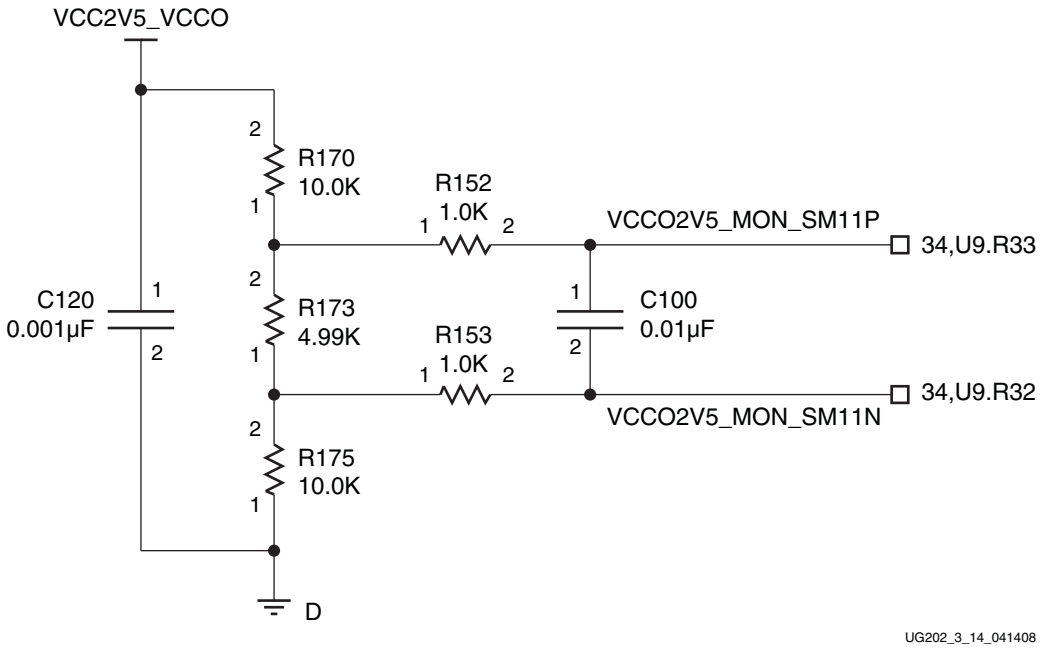

Figure 3-14: **2.5V V_{CCO} Voltage Monitor (Sheet 20)**

2.5V System Power Voltage Monitor

The signal conditioning network is shown in Figure 3-15.

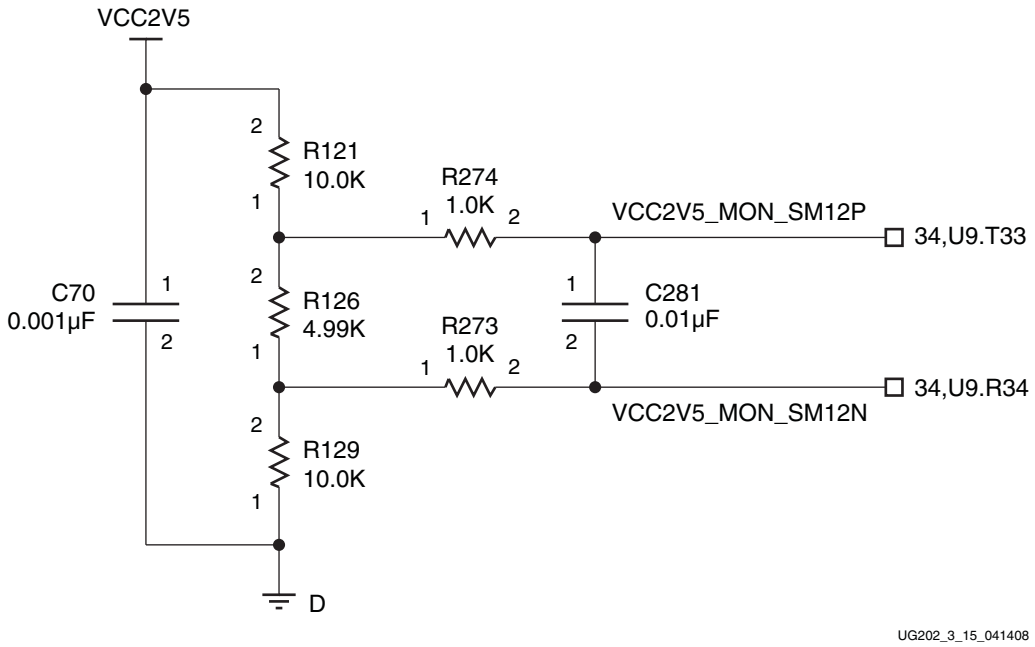

Figure 3-15: **2.5V System Power Voltage Monitor (Sheet 20)**

1.0V V_{CCINT} Voltage Monitor

The signal conditioning network is shown in Figure 3-16.

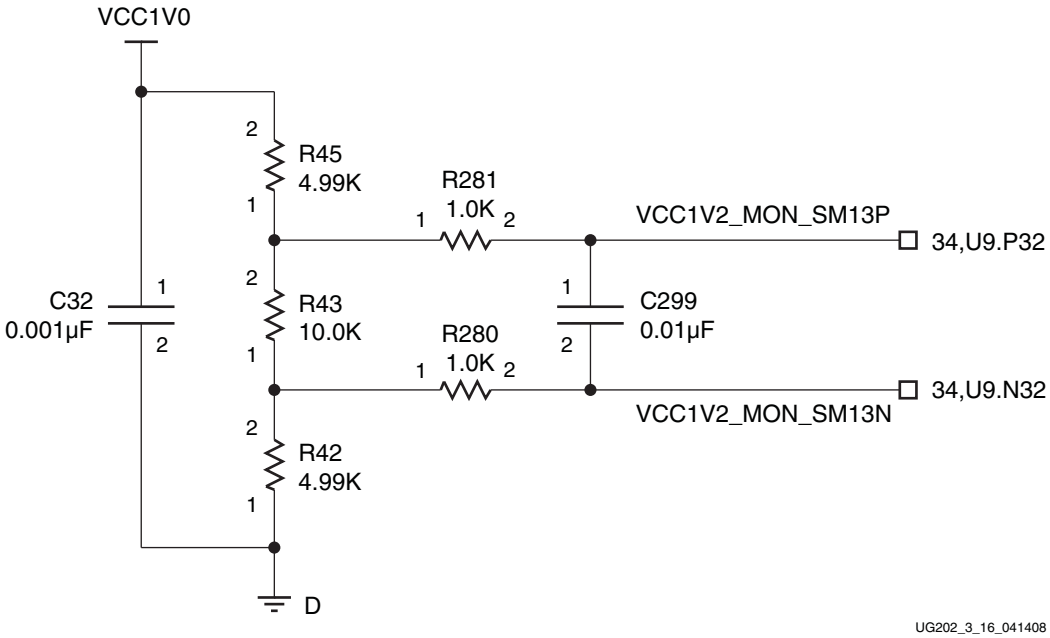

Figure 3-16: **1.0V V_{CCINT} Voltage Monitor (Sheet 20)**

5V Input Power Current Monitor

The signal conditioning network is shown in Figure 3-17.

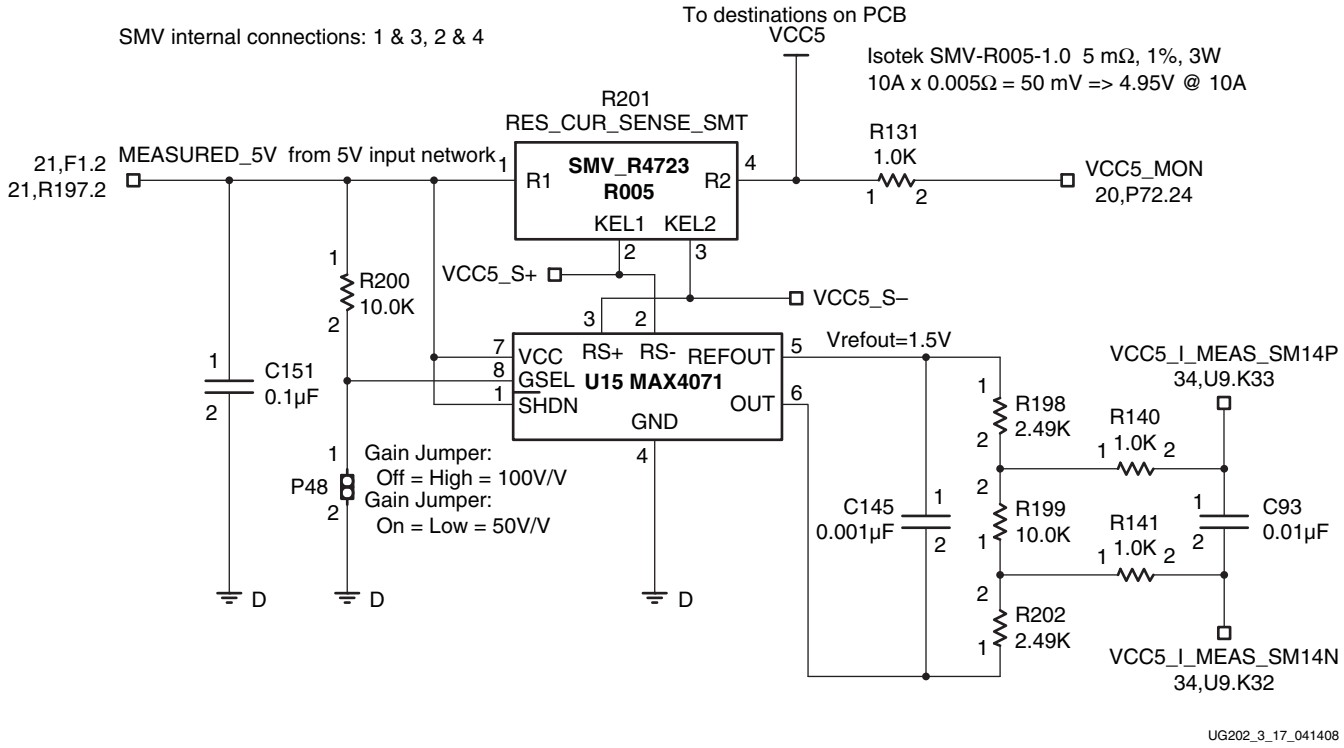

Figure 3-17: **5V Input Power Current Monitor (Sheet 19)**

PCB Temperature Monitor

The signal conditioning network is shown in Figure 3-18.

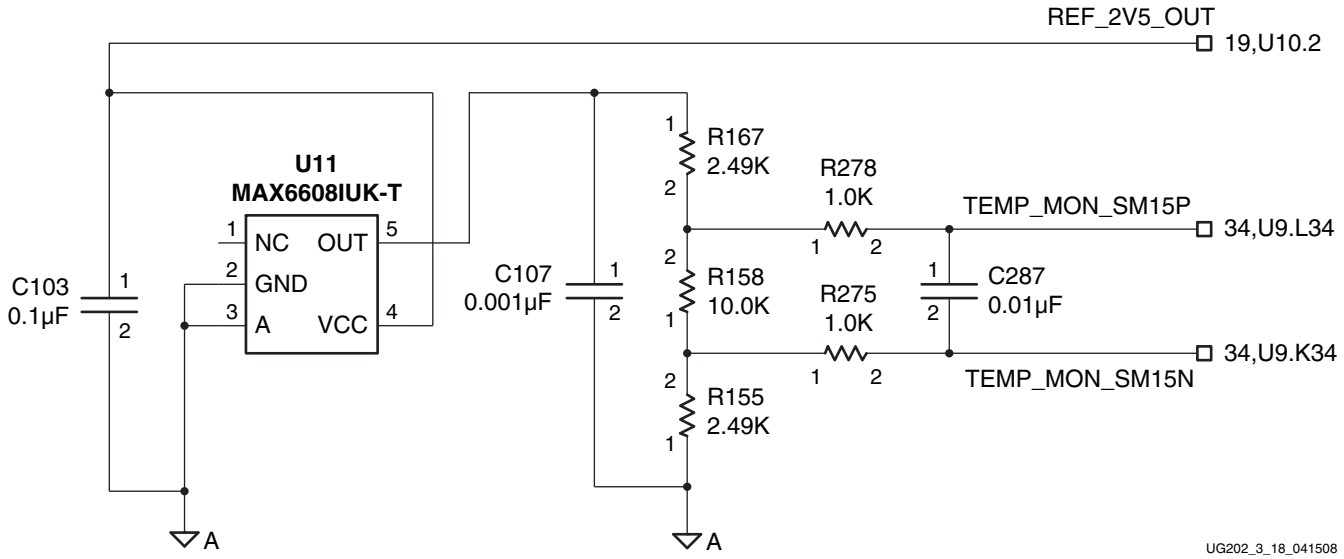

Figure 3-18: **PCB Temperature Monitor (Sheet 19)**

2.5V V_{REF} System Monitor

The signal conditioning network is shown in Figure 3-19.

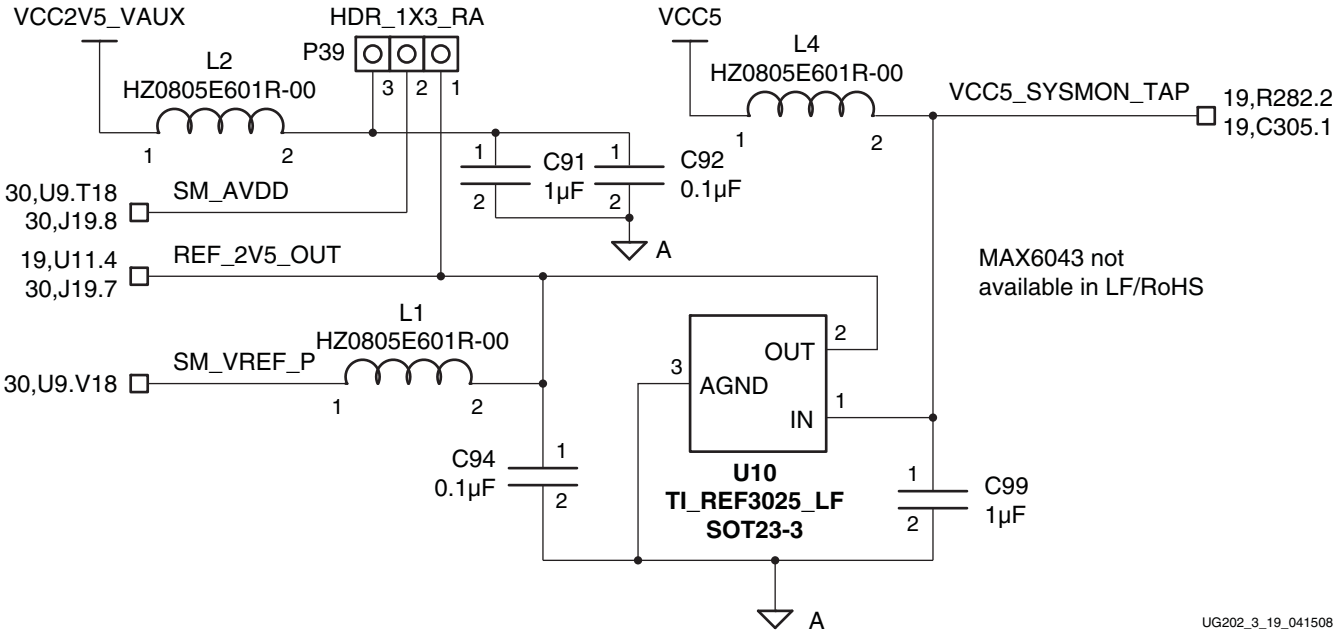

Figure 3-19: **System Monitor 2.5V Reference Selection using P39 (Sheet 19)**

P39 is a 3-pin male right-angle header with pins on 0.1-inch centers. The right-angle pins face Samtec connector P73. Depending on the length of the P39 pins, it could be difficult to install/remove the 2-pin jumper block used to select the SM_AVDD voltage on the P39.2 center pin.

To alleviate any mechanical interference between the 2-pin jumper block and the body of P73, P39 pins can be clipped shorter or bent slightly upwards to permit the 2-pin jumper block to pass above the body of P73.

P39 must be a right-angle header to keep its profile beneath the LVDS Loopback board whenever it is installed across the Samtec LVDS connectors.

System Monitor users should install the 2-pin shunt across P39 pins 1 - 2 to select the precision 2.5V U10 REF3025 output (see Table 3-14).

Table 3-14: **System Monitor 2.5V AVDD Reference Options**

P39 Pins	Selected Reference Voltage
1 - 2	U10 TI REF3025 precision 2.5V reference
2 - 3	Filtered 2.5V V_{AUX} FPGA power plane

J19 Mezzanine Board Connector

J19 is provided to enable users to develop signal conditioning boards and take advantage of the System Monitor VP/VN input channel on FPGA pins U18/V17. The J19 connections to the FPGA are shown in Figure 3-20. Four FPGA Bank 11 GPIO pins are connected to J19 to provide general purpose I/O, as detailed in Figure 3-20 and Table 3-13, page 34. J19 pinout details are shown in Table 3-15, page 42.

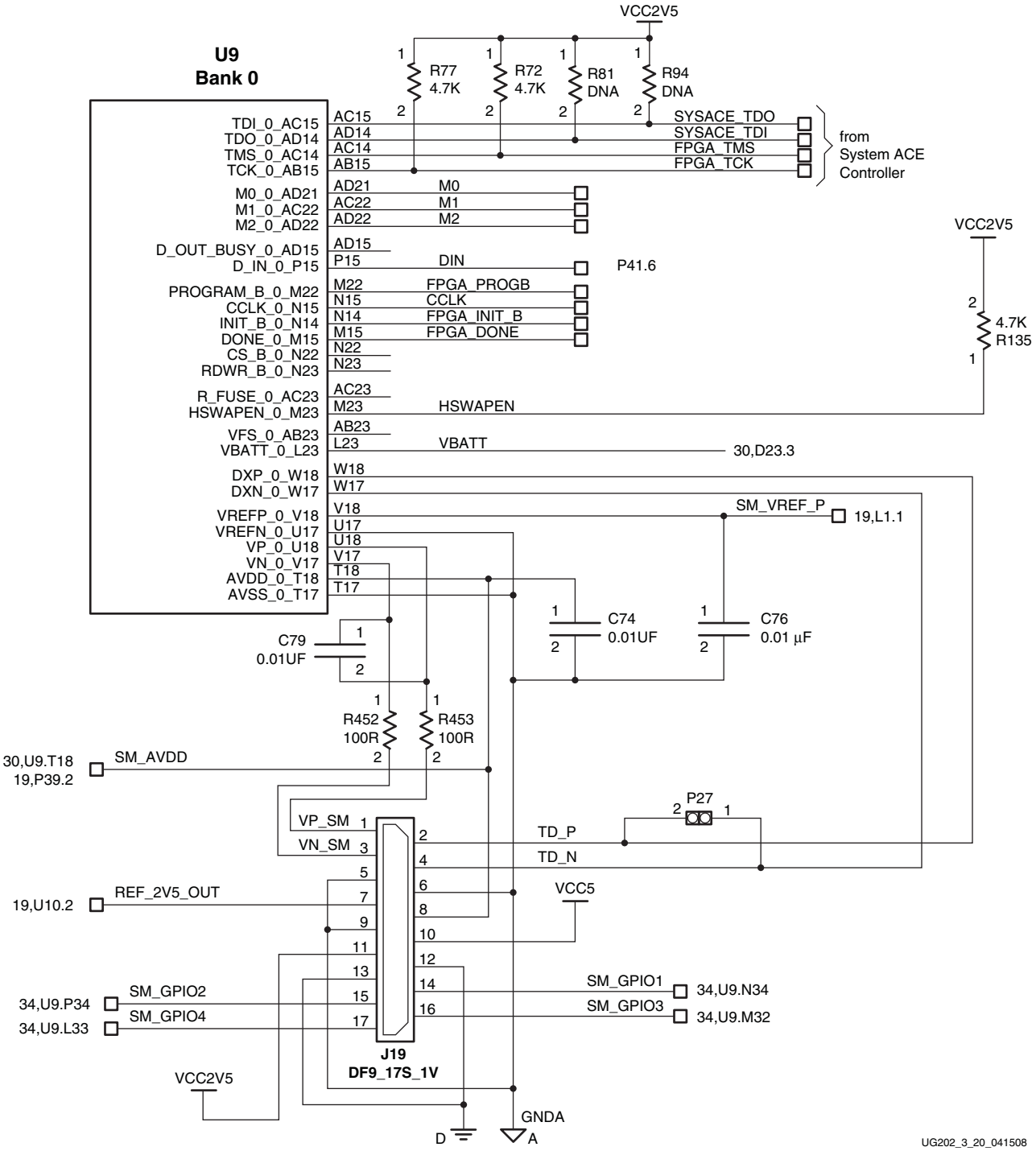

Figure 3-20: **J19 Mezzanine Board Connector (Sheet 30)**

Table 3-15: **J19 Mezzanine Board Connector**

Pin #	Signal Name	FPGA Pin #	Schematic	Notes
1	VP_SM	U18	30	Via 100Ω series resistor R453
2	TD_P	W18	30	FPGA internal temp diode DXP
3	VN_SM	V17	30	Via 100Ω series resistor R452
4	TD_N	W17	30	FPGA internal temp diode DXN
5	Agnd		30	
6	Agnd		30	
7	REF_2V5_OUT	U10.2	19, 30	U10 = REF3025 Voltage Reference
8	SM_AVDD	U9.T18, P39.2	19,30	P39 = 3-pin header (2.5V select)
9	Agnd		30	
10	VCC5		21, 30	
11	VCC2V5		22, 30	
12	Dgnd		30	
13	Dgnd		30	
14	SM_GPIO1	N34	30, 34	
15	SM_GPIO2	P34	30, 34	
16	SM_GPIO3	M32	30, 34	
17	SM_GPIO4	L33	30, 34	

Figure 3-21 shows a schematic diagram of the P72 pinouts. Refer to Table 3-16.

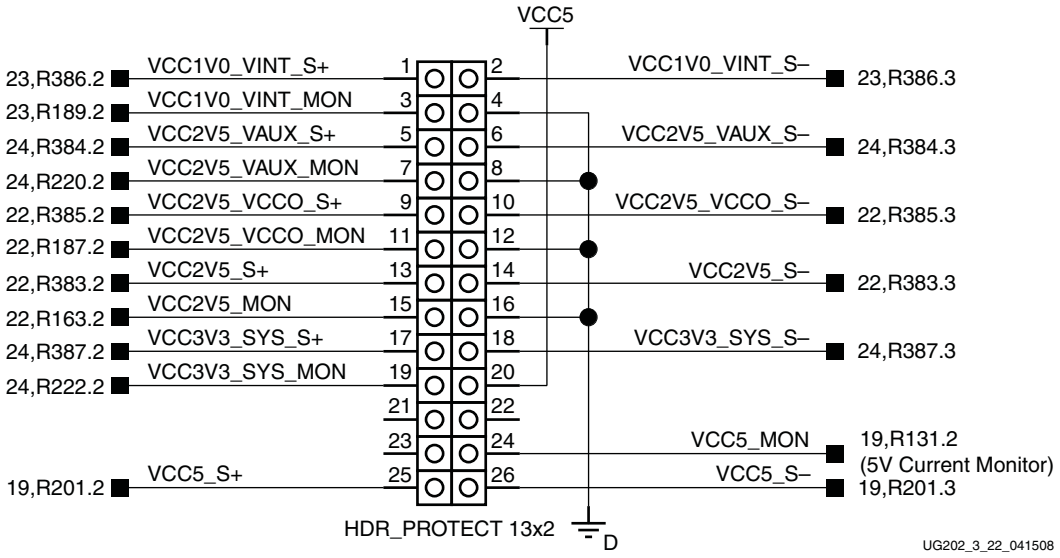

Figure 3-21: **P72 Pinout Diagram (Sheet 20)**

Power Monitor Circuitry

The ML550 hosts a 2 x 13 0.1-inch male header connector which provides test points for the ML550 power regulators as shown in Table 3-16.

Table 3-16: **Power Monitor Connector P72 Pinout**

Pin #	Signal Name	R_{KELVIN} REF	Schematic	Notes
1	VCC1V0_VINT_S+	R386	20, 23	S– actual
2	VCC1V0_VINT_S–	R386	20, 23	S+ actual
3	VCC1V0_VINT_MON	R386	20, 23	
4	Dgnd		20	
5	VCC2V5_VAUX_S+	R384	20, 24	S– actual
6	VCC2V5_VAUX_S–	R384	20, 24	S+ actual
7	VCC2V5_VAUX_MON	R384	20, 24	
8	Dgnd		20	
9	VCC2V5_VCCO_S+	R385	20, 22	S– actual
10	VCC2V5_VCCO_S–	R385	20, 22	S+ actual
11	VCC2V5_VCCO_MON	R385	20, 22	
12	Dgnd		20	
13	VCC2V5_S+	R383	20, 22	S– actual
14	VCC2V5_S–	R383	20, 22	S+ actual
15	VCC2V5_MON	R383	20, 22	
16	Dgnd		20	
17	VCC3V3_SYS_S+	R387	20, 24	S– actual
18	VCC3V3_SYS_S–	R387	20, 24	S+ actual
19	VCC3V3_SYS_MON	R387	20, 24	
20	VCC5		19, 20	
21	NC		20	
22	NC		20	
23	NC		20	
24	VCC5_MON	R201	19,20	
25	VCC5_S+	R201	19,20	S– actual
26	VCC5_S–	R201	19,20	S+ actual

The regulator outputs are connected to a series Kelvin resistor, which is then connected to the target power plane. ML550 voltage regulator topology is discussed in detail in sections "Voltage Regulators (TI PTH05000)," page 29 and "Power Monitor Connector," page 32. A summary of the regulator connections to P72 is given in Table 3-12, page 33.

Note: As indicated in Note 3 beneath Table 3-12, the S+ and S– pins of P72 are reversed.

Power Monitor Board

A small PC board (1.375 inches x 2.25 inches) is available which mates with P72 and provides two banana jacks for voltmeter probe access to V_{CCINT}, V_{CCAUX}, or V_{CCO}. See Figure 3-22.

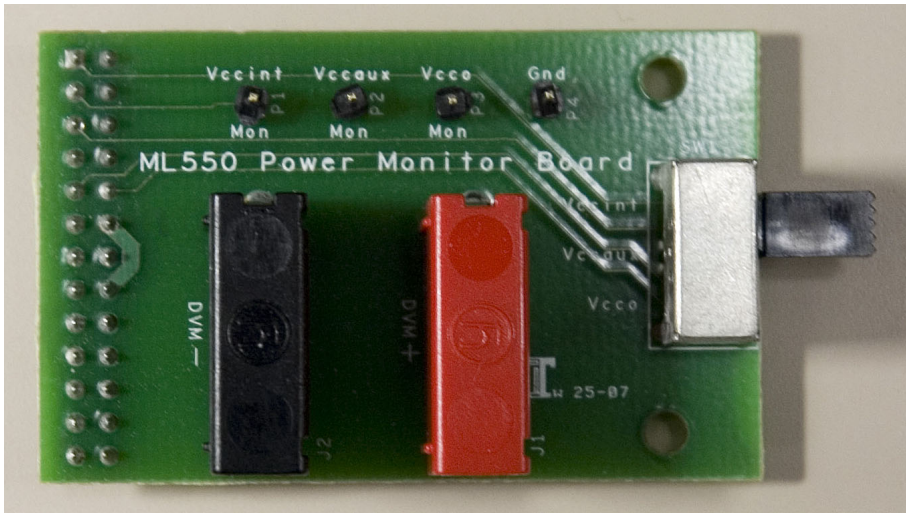

Figure 3-22: **Power Monitor Board**

Data Sheet References

Table 3-17 shows the manufacturers and part numbers of U10, U11, and U15.

Table 3-17: **IC Data Sheet References**

Reference Designator	Manufacturer	Part Number
U10	Texas Instruments	REF3025AIDBZT
U11	Maxim	MAX6608IUK+
U15	Maxim	MAX4071AUA+

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Chapter 4

Configuration

The Virtex-5 FPGA ML550 Networking Interfaces Development Board includes several options to configure the Virtex-5 FPGA. The configuration modes are:

- System ACE mode
- JTAG mode
- Slave Serial mode
- Master Serial mode

This chapter provides a brief description of the FPGA configuration methods used on the ML550 Development Board.

Configuration Modes

Table 4-1 shows the Virtex-5 FPGA configuration modes. The Master and Slave (Parallel) SelectMap configuration modes are not supported on the ML550 Development Board. Figure 4-1 shows the Configuration Mode switch (SW11).

Table 4-1: **Configuration Modes**

Mode	XCONFIG P41	JTAG P50 or P51	Mode SW11(2,3)		
			3 (M2)	2 (M1)	1 (M0)
Master Serial	X	—	0	0	0
Slave Serial	X	—	1	1	1
Master SelectMAP (1)	N/A	N/A	0	1	1
Slave SelectMAP (1)	N/A	N/A	1	1	0
JTAG	—	X	1	0	1
System ACE CF Card	—	—	1	1	1

Notes:

1. Not supported on the ML550 Networking Interfaces Platform.
2. 0 = SW11 switch position (n) is Closed.
3. 1 = SW11 switch position (n) is Open.

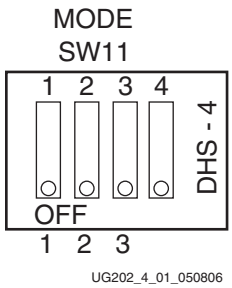

Figure 4-1: **Configuration Mode Switch**

JTAG Chain

Figure 4-2 shows the JTAG chain on the ML550 Development Board and illustrates how three different sources can be used to drive this JTAG chain. The chain can be driven by the following sources:

- System ACE controller
- Xilinx Parallel Cable IV or Platform Cable USB
- Other JTAG cables

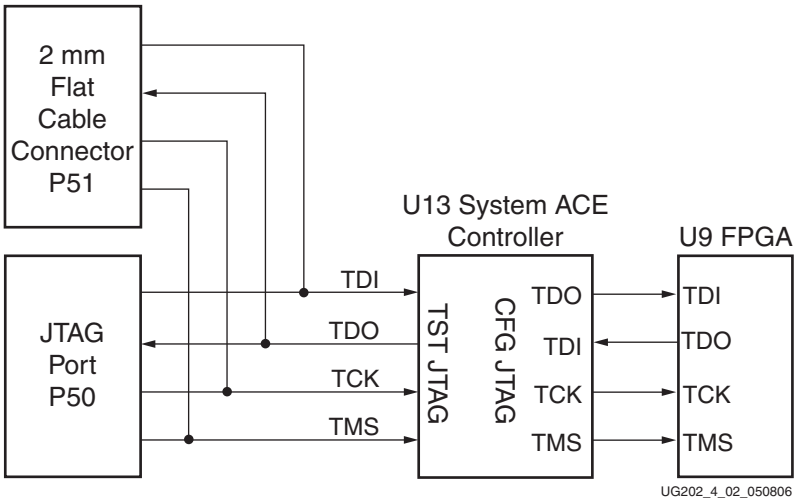

Figure 4-2: **JTAG Chain**

JTAG Ports

The ML550 Development Board provides two JTAG connectors (P50 and P51) that can be used to program the Virtex-5 FPGA. Figure 4-3 shows the pin assignments for JTAG connectors P50.

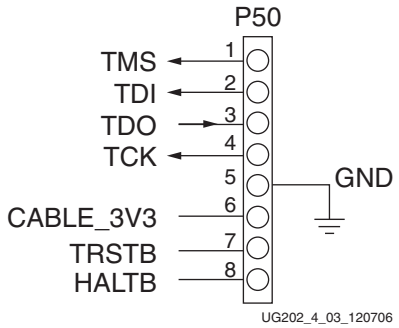

Figure 4-3: **JTAG Connector P50**

Table 4-2 describes the P50 JTAG Header signal names, descriptions, and pin assignments.

Table 4-2: **P50 JTAG Header Signal Descriptions and Pin Assignments**

Signal Name	Description	P50 Pin Number	System ACE Pin Number
TSTTDO	JTAG TDO from System ACE Interface	3	97
TSTTDI	JTAG TDI to System ACE Interface	2	102
TSTTCK	JTAG TCK to System ACE Interface	4	101
TSTTMS	JTAG TMS to System ACE Interface	1	98
HALTB	User Defined	8	N/A; goes to FPGA pin AG5
TRSTB	User Defined	7	N/A; goes to FPGA pin AF5

2 mm Flat Cable Port

The ML550 Development Board provides a 2 mm flat cable connector (P51) to configure the Virtex-5 FPGA. Figure 4-4 shows the pin assignments for the 2 mm flat cable connector. The 2 mm flat cable connector can also be used to configure the FPGA in Slave Serial configuration mode.

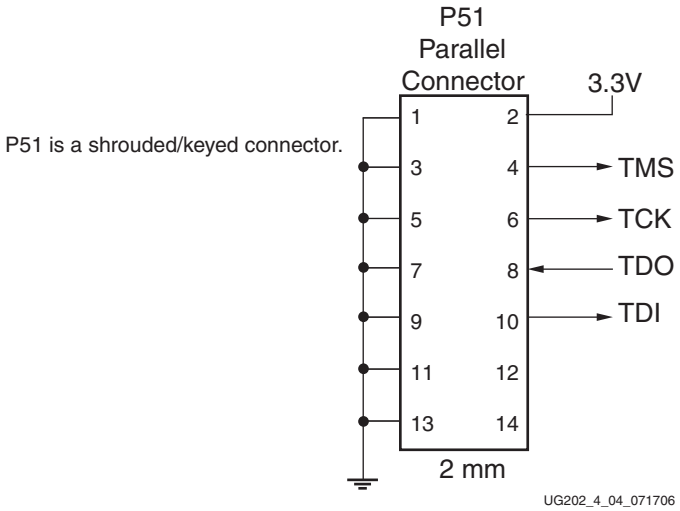

Figure 4-4: **2 mm Flat Cable Connector P51**

System ACE Interface

The ML550 Development Board provides a System ACE interface to configure the Virtex-5 FPGA. The interface also gives software designers the ability to run code (for soft processor IP within the FPGA) from removable CompactFlash cards. Figure 4-5 shows the System ACE interface. When the MPU port of the System ACE Controller is used, the Virtex-5 FPGA and the System ACE Controller use the same clock source for interface synchronization.

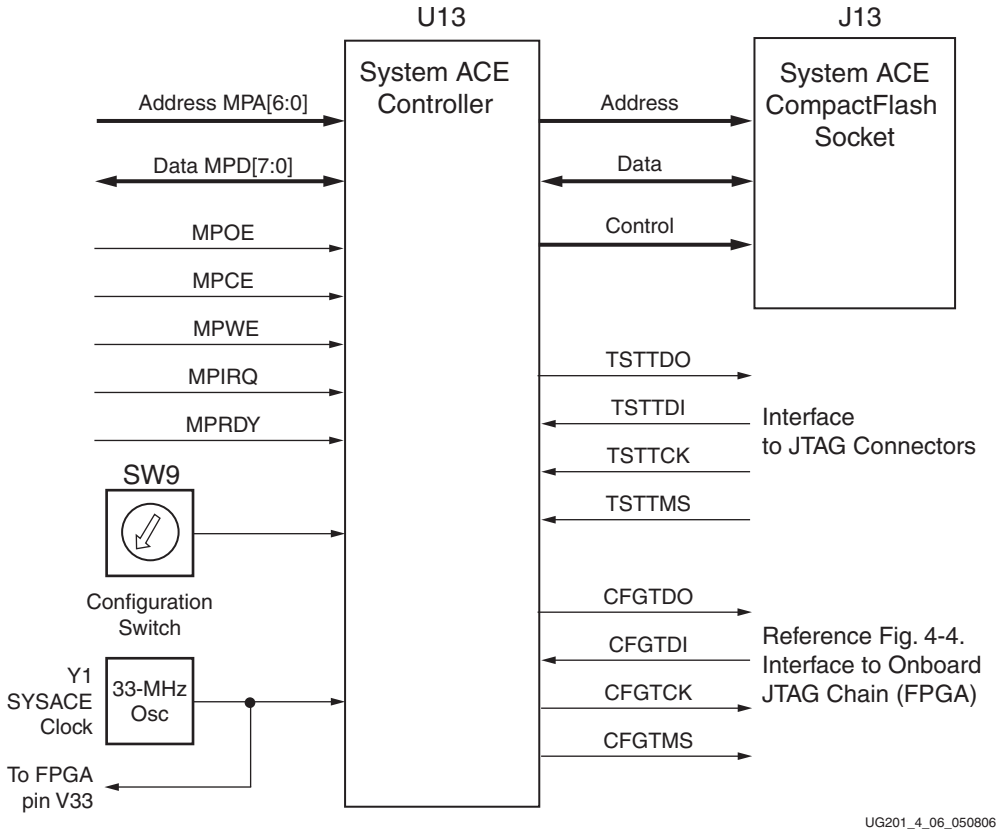

Figure 4-5: **System ACE Interface**

For detailed information on creation of System ACE compatible ACE files, formatting the CF card, and storing multiple design images, see the System ACE CompactFlash Solution Advance Product Specification (DS080) at:

http://www.xilinx.com/support/documentation/data_sheets/ds080.pdf

Table 4-3 shows the System ACE interface signal names, descriptions, and pin assignments.

Table 4-3: **System ACE Interface Signal Descriptions**

System ACE Pin Number	Signal Name	FPGA Pin Number
70	SYSACE_MPA0	AB33
69	SYSACE_MPA1	AC33
68	SYSACE_MPA2	AB32
67	SYSACE_MPA3	AC32
45	SYSACE_MPA4	AD34
44	SYSACE_MPA5	AC34
43	SYSACE_MPA6	W32
66	SYSACE_MPD0	AE32
65	SYSACE_MPD1	AD32
63	SYSACE_MPD2	AJ34
62	SYSACE_MPD3	AH34
61	SYSACE_MPD4	AE34
60	SYSACE_MPD5	AF34
59	SYSACE_MPD6	AE33
58	SYSACE_MPD7	AF33
77	SYSACE_CTRL0/MPOE	Y32
76	SYSACE_CTRL1/MPWE	Y34
42	SYSACE_CTRL2/MPCE	AA34
41	SYSACE_CTRL3/MPIRQ	AA33
39	SYSACE_CTRL4/MPBRDY	Y33
93	SYSACE_CLK	V33

Appendix A

LVDS

This appendix provides the pinouts for the six LVDS connectors.

LVDS Transmit Connectors

Table A-1 lists the connections for LVDS transmit connector #1 (P73), Table A-2 lists the connections for LVDS transmit connector #2 (P46), and Table A-3 lists the connections for LVDS transmit connector #3 (P49). These connectors and their associated FPGA banks are detailed on ML550 0381218 schematic pages 6, 7, and 8.

The clock multiplier U16 connections are shown in Table A-2 and associated with P46 on schematic page 7. The multiply and divide circuitry (detailed on schematic sheet 12) is discussed in "LVDS Connectors," page 28.

Table A-1: **LVDS Transmit Connector #1 (P73)**

P73 Pin #	TX Signal Name	U9 Pin #	U9 Bank #	P73 Pin #	TX Signal Name	U9 Pin #	U9 Bank #
1	NC			45	GND		
2	NC			46	GND		
3	NC			47	LVDS_DATAOUT_11N	W26	17
4	NC			48	LVDS_DATAOUT_CLKCAP_10N	Y29	17
5	GND			49	LVDS_DATAOUT_11P	Y26	17
6	GND			50	LVDS_DATAOUT_CLKCAP_10P	Y28	17
7	NC			51	GND		
8	NC			52	GND		
9	NC			53	LVDS_DATAOUT_CLKCAP_09N	AA31	17
10	NC			54	LVDS_DATAOUT_CLKCAP_08N	AA30	17
11	GND			55	LVDS_DATAOUT_CLKCAP_09P	AB31	17
12	GND			56	LVDS_DATAOUT_CLKCAP_08P	AA29	17
13	NC			57	GND		
14	NC			58	GND		
15	NC			59	LVDS_DATAOUT_07N	AC29	17
16	NC			60	LVDS_DATAOUT_06N	AF30	17

Table A-1: **LVDS Transmit Connector #1 (P73) *(Continued)***

P73 Pin #	TX Signal Name	U9 Pin #	U9 Bank #	P73 Pin #	TX Signal Name	U9 Pin #	U9 Bank #
17	GND			61	LVDS_DATAOUT_07P	AD30	17
18	GND			62	LVDS_DATAOUT_06P	AF29	17
19	NC			63	GND		
20	NC			64	GND		
21	NC			65	LVDS_DATAOUT_05N	AE31	17
22	NC			66	LVDS_DATAOUT_04N	AD29	17
23	GND			67	LVDS_DATAOUT_05P	AD31	17
24	GND			68	LVDS_DATAOUT_04P	AE29	17
25	NC			69	GND		
26	LVDS_DATAOUT_18N	V27	17	70	GND		
27	NC			71	LVDS_DATAOUT_03N	AG31	17
28	LVDS_DATAOUT_18P	V28	17	72	LVDS_DATAOUT_02N	AK31	17
29	GND			73	LVDS_DATAOUT_03P	AF31	17
30	GND			74	LVDS_DATAOUT_02P	AJ31	17
31	LVDS_DATAOUT_17N	V24	17	75	GND		
32	LVDS_DATAOUT_16N	V29	17	76	GND		
33	LVDS_DATAOUT_17P	W24	17	77	LVDS_DATAOUT_01N	AH30	17
34	LVDS_DATAOUT_16P	W29	17	78	LVDS_DATAOUT_00N	AG30	17
35	GND			79	LVDS_DATAOUT_01P	AJ30	17
36	GND			80	LVDS_DATAOUT_00P	AH29	17
37	LVDS_DATAOUT_15N	W25	17	81	GND		
38	LVDS_DATAOUT_14N	W27	17	82	GND		
39	LVDS_DATAOUT_15P	V25	17	83	GND		
40	LVDS_DATAOUT_14P	Y27	17	84	GND		
41	LVDS_DATAOUT_13N	Y31	17	85	GND		
42	LVDS_DATAOUT_12N	W30	17	86	GND		
43	LVDS_DATAOUT_13P	W31	17	87	GND		
44	LVDS_DATAOUT_12P	V30	17	88	GND		

Table A-2: **LVDS Transmit Connector #2 (P46)**

P46 Pin #	TX Signal Name	U9 Pin #	U9 Bank #	P46 Pin #	TX Signal Name	U9 Pin #	U9 Bank #
1	NC			45	GND		
2	NC			46	GND		
3	NC			47	LVDS_DATAOUT_29N	AE26	21
4	NC			48	LVDS_DATAOUT_30N	AC24	21
5	GND			49	LVDS_DATAOUT_29P	AE27	21
6	GND			50	LVDS_DATAOUT_30P	AC25	21
7	NC			51	GND		
8	NC			52	GND		
9	NC			53	LVDS_DATAOUT_CLKCAP_27N	AJ29	21
10	NC			54	LVDS_DATAOUT_28N	AD25	21
11	GND			55	LVDS_DATAOUT_CLKCAP_27P	AK29	21
12	GND			56	LVDS_DATAOUT_28P	AD26	21
13	NC			57	GND		
14	NC			58	GND		
15	NC			59	LVDS_DATAOUT_25N	AH28	21
16	NC			60	LVDS_DATAOUT_26N	AE24	21
17	GND			61	LVDS_DATAOUT_25P	AG28	21
18	GND			62	LVDS_DATAOUT_26P	AD24	21
19	NC			63	GND		
20	NC			64	GND		
21	NC			65	LVDS_DATAOUT_23N	AF28	21
22	NC			66	LVDS_DATAOUT_24N	AF26	21
23	GND			67	LVDS_DATAOUT_23P	AE28	21
24	GND			68	LVDS_DATAOUT_24P	AF25	21
25	GCLK_TX_N	AJ27	21	69	GND		
26	NC			70	GND		
27	GCLK_TX_P	AK26	21	71	LVDS_DATAOUT_21N	AG26	21
28	NC			72	LVDS_DATAOUT_22N	AA26	21
29	GND			73	LVDS_DATAOUT_21P	AG27	21
30	GND			74	LVDS_DATAOUT_22P	AA25	21
31	LVDS_DATAOUT_35N	AA28	21	75	GND		
32	XMITCLK_N	12	U16	76	GND		

Table A-2: **LVDS Transmit Connector #2 (P46) *(Continued)***

P46 Pin #	TX Signal Name	U9 Pin #	U9 Bank #	P46 Pin #	TX Signal Name	U9 Pin #	U9 Bank #
33	LVDS_DATAOUT_35P	AB28	21	77	LVDS_DATAOUT_19N	AH25	21
34	XMITCLK_P	13	U16	78	LVDS_DATAOUT_20N	AG25	21
35	GND			79	LVDS_DATAOUT_19P	AJ25	21
36	GND			80	LVDS_DATAOUT_20P	AF24	21
37	LVDS_DATAOUT_33N	AC27	21	81	GND		
38	LVDS_DATAOUT_34N	AA24	21	82	GND		
39	LVDS_DATAOUT_33P	AB27	21	83	GND		
40	LVDS_DATAOUT_34P	Y24	21	84	GND		
41	LVDS_DATAOUT_31N	AD27	21	85	GND		
42	LVDS_DATAOUT_32N	AB26	21	86	GND		
43	LVDS_DATAOUT_31P	AC28	21	87	GND		
44	LVDS_DATAOUT_32P	AB25	21	88	GND		

Table A-3: **LVDS Transmit Connector #3 (P49)**

P49 Pin #	TX Signal Name	U9 Pin #	U9 Bank #	P49 Pin #	TX Signal Name	U9 Pin #	U9 Bank #
1	NC			45	GND		
2	NC			46	GND		
3	NC			47	LVDS_DATAOUT_45N	AM11	22
4	NC			48	LVDS_DATAOUT_46N	AC9	22
5	GND			49	LVDS_DATAOUT_45P	AM12	22
6	GND			50	LVDS_DATAOUT_46P	AC10	22
7	NC			51	GND		
8	NC			52	GND		
9	NC			53	LVDS_DATAOUT_43N	AE11	22
10	NC			54	LVDS_DATAOUT_CLKCAP_44N	AJ11	22
11	GND			55	LVDS_DATAOUT_43P	AF11	22
12	GND			56	LVDS_DATAOUT_CLKCAP_44P	AK11	22
13	NC			57	GND		
14	NC			58	GND		
15	NC			59	LVDS_DATAOUT_41N	AH10	22
16	NC			60	LVDS_DATAOUT_42N	AF10	22
17	GND			61	LVDS_DATAOUT_41P	AH9	22

Table A-3: **LVDS Transmit Connector #3 (P49) *(Continued)***

P49 Pin #	TX Signal Name	U9 Pin #	U9 Bank #	P49 Pin #	TX Signal Name	U9 Pin #	U9 Bank #
18	GND			62	LVDS_DATAOUT_42P	AF9	22
19	NC			63	GND		
20	NC			64	GND		
21	NC			65	LVDS_DATAOUT_39N	AJ10	22
22	NC			66	LVDS_DATAOUT_40N	AE9	22
23	GND			67	LVDS_DATAOUT_39P	AJ9	22
24	GND			68	LVDS_DATAOUT_40P	AF8	22
25	NC			69	GND		
26	NC			70	GND		
27	NC			71	LVDS_DATAOUT_37N	AK9	22
28	NC			72	LVDS_DATAOUT_38N	AG11	22
29	GND			73	LVDS_DATAOUT_37P	AK8	22
30	GND			74	LVDS_DATAOUT_38P	AG10	22
31	LVDS_DATAOUT_51N	AP14	22	75	GND		
32	LVDS_DATAOUT_52N	AA10	22	76	GND		
33	LVDS_DATAOUT_51P	AN14	22	77	NC		
34	LVDS_DATAOUT_52P	AB10	22	78	LVDS_DATAOUT_36N	AH8	22
35	GND			79	NC		
36	GND			80	LVDS_DATAOUT_36P	AG8	22
37	LVDS_DATAOUT_49N	AM13	22	81	GND		
38	LVDS_DATAOUT_50N	AA9	22	82	GND		
39	LVDS_DATAOUT_49P	AN13	22	83	GND		
40	LVDS_DATAOUT_50P	AA8	22	84	GND		
41	LVDS_DATAOUT_47N	AN12	22	85	GND		
42	LVDS_DATAOUT_48N	AB8	22	86	GND		
43	LVDS_DATAOUT_47P	AP12	22	87	GND		
44	LVDS_DATAOUT_48P	AC8	22	88	GND		

LVDS Receive Connectors

Table A-4 lists the connections for LVDS receive connector #1 (P74), Table A-5 lists the connections for LVDS receive connector #2 (P6), and Table A-6 lists the connections for LVDS receive connector #3 (P3). These connectors and their associated FPGA banks are detailed on ML550 0381218 schematic pages 9, 10, and 11.

The clock divider U17 connections are shown in Table A-5 and associated with P6 on schematic page 10. The multiply and divide circuitry (detailed on schematic sheet 12) is discussed in "LVDS Connectors," page 28.

Table A-4: **LVDS Receive Connector #1 (P74)**

P74 Pin #	RX Signal Name	U9 Pin #	U9 Bank #	P74 Pin #	RX Signal Name	U9 Pin #	U9 Bank #
1	LVDS_DATAIN_00P	H30	15	45	GND		15
2	LVDS_DATAIN_01P	F31	15	46	GND		
3	LVDS_DATAIN_00N	G31	15	47	LVDS_DATAIN_16P	U30	15
4	LVDS_DATAIN_01N	E31	15	48	LVDS_DATAIN_17P	H29	15
5	GND			49	LVDS_DATAIN_16N	T30	15
6	GND			50	LVDS_DATAIN_17N	J29	15
7	LVDS_DATAIN_02P	U25	15	51	GND		
8	LVDS_DATAIN_03P	J30	15	52	NC		
9	LVDS_DATAIN_02N	T25	15	53	LVDS_DATAIN_18P	G30	15
10	LVDS_DATAIN_03N	J31	15	54	NC		
11	GND			55	LVDS_DATAIN_18N	F30	15
12	GND			56	GND		
13	LVDS_DATAIN_04P	U26	15	57	NC		
14	LVDS_DATAIN_05P	R26	15	58	NC		
15	LVDS_DATAIN_04N	T26	15	59	NC		
16	LVDS_DATAIN_05N	R27	15	60	NC		
17	GND			61	GND		
18	GND			62	GND		
19	LVDS_DATAIN_06P	L29	15	63	NC		
20	LVDS_DATAIN_07P	U27	15	64	NC		
21	LVDS_DATAIN_06N	K29	15	65	NC		
22	LVDS_DATAIN_07N	U28	15	66	NC		
23	GND			67	GND		
24	GND			68	GND		
25	LVDS_DATAIN_CLKCAP_08P	M31	15	69	NC		
26	LVDS_DATAIN_CLKCAP_09P	P31	15	70	NC		

Table A-4: **LVDS Receive Connector #1 (P74) *(Continued)***

P74 Pin #	RX Signal Name	U9 Pin #	U9 Bank #	P74 Pin #	RX Signal Name	U9 Pin #	U9 Bank #
27	LVDS_DATAIN_CLKCAP_08N	N30	15	71	NC		
28	LVDS_DATAIN_CLKCAP_09N	P30	15	72	NC		
29	GND			73	GND		
30	GND			74	GND		
31	LVDS_DATAIN_CLKCAP_10P	K31	15	75	NC		
32	LVDS_DATAIN_CLKCAP_11P	N29	15	76	NC		
33	LVDS_DATAIN_CLKCAP_10N	L31	15	77	NC		
34	LVDS_DATAIN_CLKCAP_11N	P29	15	78	NC		
35	GND			79	GND		
36	GND			80	GND		
37	LVDS_DATAIN_12P	L30	15	81	GND		
38	LVDS_DATAIN_13P	R28	15	82	GND		
39	LVDS_DATAIN_12N	M30	15	83	GND		
40	LVDS_DATAIN_13N	R29	15	84	GND		
41	LVDS_DATAIN_14P	T31	15	85	GND		
42	LVDS_DATAIN_15P	T28	15	86	GND		
43	LVDS_DATAIN_14N	R31	15	87	GND		
44	LVDS_DATAIN_15N	T29	15	88	GND		

Table A-5: **LVDS Receive Connector #2 (P6)**

P6 Pin #	RX Signal Name	U9 Pin #	U9 Bank #	P6 Pin #	RX Signal Name	U9 Pin #	U9 Bank #
1	LVDS_DATAIN_20P	N27	19	45	GND		
2	LVDS_DATAIN_19P	N24	19	46	GND		
3	LVDS_DATAIN_20N	M27	19	47	RCVCLK_P	2	U17
4	LVDS_DATAIN_19N	P24	19	48	LVDS_DATAIN_35P	F25	19
5	GND			49	RCVCLK_N	3	U17
6	GND			50	LVDS_DATAIN_35N	F26	19
7	LVDS_DATAIN_22P	K28	19	51	GND		
8	LVDS_DATAIN_21P	P25	19	52	GND		
9	LVDS_DATAIN_22N	L28	19	53	NC		
10	LVDS_DATAIN_21N	N25	19	54	GCLK_RX_P	J14	3
11	GND			55	NC		

Table A-5: **LVDS Receive Connector #2 (P6) *(Continued)***

P6 Pin #	RX Signal Name	U9 Pin #	U9 Bank #	P6 Pin #	RX Signal Name	U9 Pin #	U9 Bank #
12	GND			56	GCLK_RX_N	H13	3
13	LVDS_DATAIN_24P	J24	19	57	GND		
14	LVDS_DATAIN_23P	J27	19	58	GND		
15	LVDS_DATAIN_24N	J25	19	59	NC		
16	LVDS_DATAIN_23N	J26	19	60	NC		
17	GND			61	NC		
18	GND			62	NC		
19	LVDS_DATAIN_26P	G25	19	63	GND		
20	LVDS_DATAIN_25P	H25	19	64	GND		
21	LVDS_DATAIN_26N	G26	19	65	NC		
22	LVDS_DATAIN_25N	H24	19	66	NC		
23	GND			67	NC		
24	GND			68	NC		
25	LVDS_DATAIN_CLKCAP_28P	H28	19	69	GND		
26	LVDS_DATAIN_CLKCAP_27P	E26	19	70	GND		
27	LVDS_DATAIN_CLKCAP_28N	G28	19	71	NC		
28	LVDS_DATAIN_CLKCAP_27N	E27	19	72	NC		
29	GND			73	NC		
30	GND			74	NC		
31	LVDS_DATAIN_30P	K27	19	75	GND		
32	LVDS_DATAIN_CLKCAP_29P	G27	19	76	GND		
33	LVDS_DATAIN_30N	K26	19	77	NC		
34	LVDS_DATAIN_CLKCAP_29N	H27	19	78	NC		
35	GND			79	NC		
36	GND			80	NC		
37	LVDS_DATAIN_32P	P26	19	81	GND		
38	LVDS_DATAIN_31P	R24	19	82	GND		
39	LVDS_DATAIN_32N	P27	19	83	GND		
40	LVDS_DATAIN_31N	T24	19	84	GND		
41	LVDS_DATAIN_34P	M25	19	85	GND		
42	LVDS_DATAIN_33P	M28	19	86	GND		

Table A-5: **LVDS Receive Connector #2 (P6) *(Continued)***

P6 Pin #	RX Signal Name	U9 Pin #	U9 Bank #	P6 Pin #	RX Signal Name	U9 Pin #	U9 Bank #
43	LVDS_DATAIN_34N	M26	19	87	GND		
44	LVDS_DATAIN_33N	N28	19	88	GND		

Table A-6: **LVDS Receive Connector #3 (P3)**

P3 Pin #	RX Signal Name	U9 Pin #	U9 Bank #	P3 Pin #	RX Signal Name	U9 Pin #	U9 Bank #
1	LVDS_DATAIN_36P	E9	20	45	GND		
2	NC			46	GND		
3	LVDS_DATAIN_36N	E8	20	47	LVDS_DATAIN_52P	K11	20
4	NC			48	LVDS_DATAIN_51P	N10	20
5	GND			49	LVDS_DATAIN_52N	J11	20
6	GND			50	LVDS_DATAIN_51N	N9	20
7	LVDS_DATAIN_38P	F11	20	51	GND		
8	LVDS_DATAIN_37P	F9	20	52	GND		
9	LVDS_DATAIN_38N	E11	20	53	NC		
10	LVDS_DATAIN_37N	F8	20	54	NC		
11	GND			55	NC		
12	GND			56	NC		
13	LVDS_DATAIN_40P	D11	20	57	GND		
14	LVDS_DATAIN_39P	F10	20	58	GND		
15	LVDS_DATAIN_40N	D10	20	59	NC		
16	LVDS_DATAIN_39N	G10	20	60	NC		
17	GND			61	NC		
18	GND			62	NC		
19	LVDS_DATAIN_42P	G11	20	63	GND		
20	LVDS_DATAIN_41P	G8	20	64	GND		
21	LVDS_DATAIN_42N	G12	20	65	NC		
22	LVDS_DATAIN_41N	H8	20	66	NC		
23	GND			67	NC		
24	GND			68	NC		
25	LVDS_DATAIN_CLKCAP_44P	K8	20	69	GND		
26	LVDS_DATAIN_CLKCAP_43P	B13	20	70	GND		
27	LVDS_DATAIN_CLKCAP_44N	K9	20	71	NC		

Table A-6: **LVDS Receive Connector #3 (P3) *(Continued)***

P3 Pin #	RX Signal Name	U9 Pin #	U9 Bank #	P3 Pin #	RX Signal Name	U9 Pin #	U9 Bank #
28	LVDS_DATAIN_CLKCAP_43N	C13	20	72	NC		
29	GND			73	NC		
30	GND			74	NC		
31	LVDS_DATAIN_46P	D12	20	75	GND		
32	LVDS_DATAIN_45P	H10	20	76	GND		
33	LVDS_DATAIN_46N	C12	20	77	NC		
34	LVDS_DATAIN_45N	H9	20	78	NC		
35	GND			79	NC		
36	GND			80	NC		
37	LVDS_DATAIN_48P	E12	20	81	GND		
38	LVDS_DATAIN_47P	L10	20	82	GND		
39	LVDS_DATAIN_48N	E13	20	83	GND		
40	LVDS_DATAIN_47N	L11	20	84	GND		
41	LVDS_DATAIN_50P	M8	20	85	GND		
42	LVDS_DATAIN_49P	M10	20	86	GND		
43	LVDS_DATAIN_50N	L8	20	87	GND		
44	LVDS_DATAIN_49N	L9	20	88	GND		

Appendix B

LVDS Loopback Board

The Xilinx LVDS Loopback board (P/N 0431395) is an ML550 accessory board that bridges the ML550 LVDS Transmit and Receive Samtec connectors. Figure B-1 is a photograph of the board.

UG202_B_01_050906

Figure B-1: **Xilinx LVDS Loopback Board**

The specifications for the loopback board are:

- Dimensions are 2.25 inches by 7.00 inches
- 10 layers
- RoHS Polyclad 370HR material (FR4 equivalent)
- Silver immersion finish
- 75 mil thickness
- 100 Ω ±10% differential signal pair impedance
- Trace length specification is matched 25± ps
- Base trace length rule is a minimum of 6439 mils and a maximum of 6527 mils, with a delta of 88 mils
- Propagation delay is 1 ps per 5.71428 mils
- Actual trace is minimum of 1126.825 ps and a maximum of 1142.225 ps
- Trace-to-trace maximum delay differential is 15.400 ps
- Trace length specification is 6483 mils ± 44 mils
- Delay specification is 1134.526 ps ± 7.700 ps

Appendix C

LCD Interface

This appendix is extracted from the *XLVDSPRO Demonstration Boards User Guide* (UG037). It describes the LCD interface for the XLVDSPRO demonstration boards, which is identical to that used in the ML550 Development Board. The documentation is reproduced here for convenience.

General

The XlvdsPro_PwrIo board has a full graphical LCD display. This display has been chosen because of its possible use in embedded systems. A character-type display also can be connected because the graphical LCD used has the same interface as all character-type LCD panels.

A hardware character generator must be designed in order to display characters on the screen.

Display Hardware Design

The FPGA (I/O functioning at 2.5V) is connected to the graphic LCD display through a set of voltage-level converting devices. These switches translate the 2.5 I/O voltage to a 3.3V voltage for the LCD display.

To use the display, DIP switch 4 of the switch array DIP1 must be closed. When this switch is open, the I/O used for the LCD can be used for other applications through the SamArray connectors.

A graphics-based LCD panel from DisplayTech (64128EFCBC-XLP) is used on the Virtex-II Pro FPGA board. The control for this LCD panel is based on the KS0713 controller from Samsung. The KS0713 is a 65-column, 132-segment driver-controller device for graphic dot matrix LCD display systems. The chip accepts serial or parallel display data. The 8-bit parallel interface is compatible with most LCD panel manufacturers. The serial connection mode is write only.

Extra features added to the interface in addition to the normal parallel signals are:

- Intel or Motorola compatible interface
- External reset of the chip
- External chip select

The interface also contains the following built-in options for the display and controller:

- On-chip oscillator circuitry
- On-chip voltage converter (x2, x3, x4, and x5)
- A 64-step electronic contrast control function

Table C-1 summarizes the controller specifications.

Table C-1: **Display Controller Specifications**

Parameter	Specification
Supply voltage	2.4V to 3.6V (V_{DD})
LCD driving voltage	4V to 15V (V_{LCD} = V0 - V_{DD})
Power consumption	70µA typical (V_{DD} = 3V, x4 boost, V0 = 11V, internal supply = ON)
Sleep mode	2µA
Standby mode	10µA

The on-chip RAM size is 65x132 = 8580 bits.

Hardware Schematic Diagram

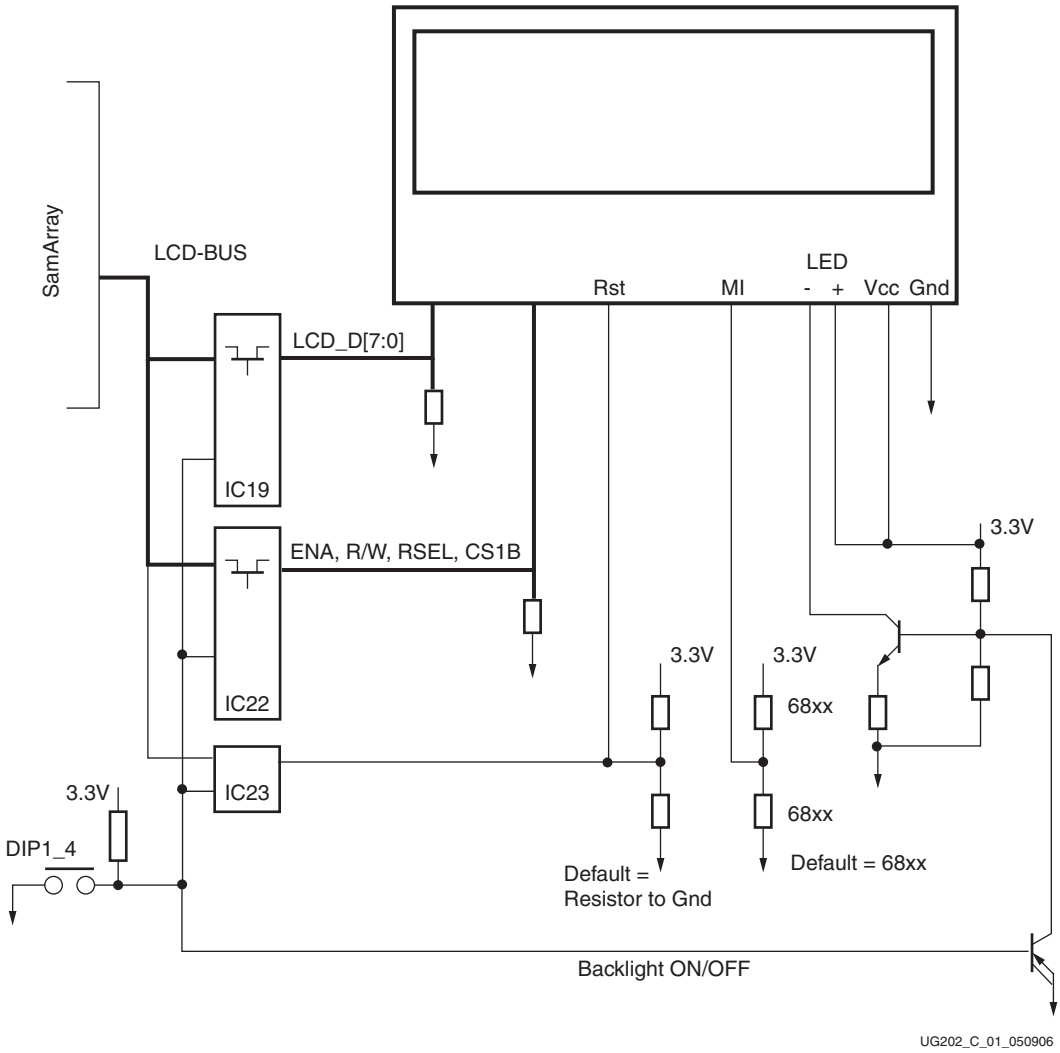

Figure C-1: **Display Schematic Diagram**

Peripheral Device KS0713

Figure C-2 shows only the signals of interest for the LCD controller. Download the data sheet from the Samsung web pages for a complete signal listing.

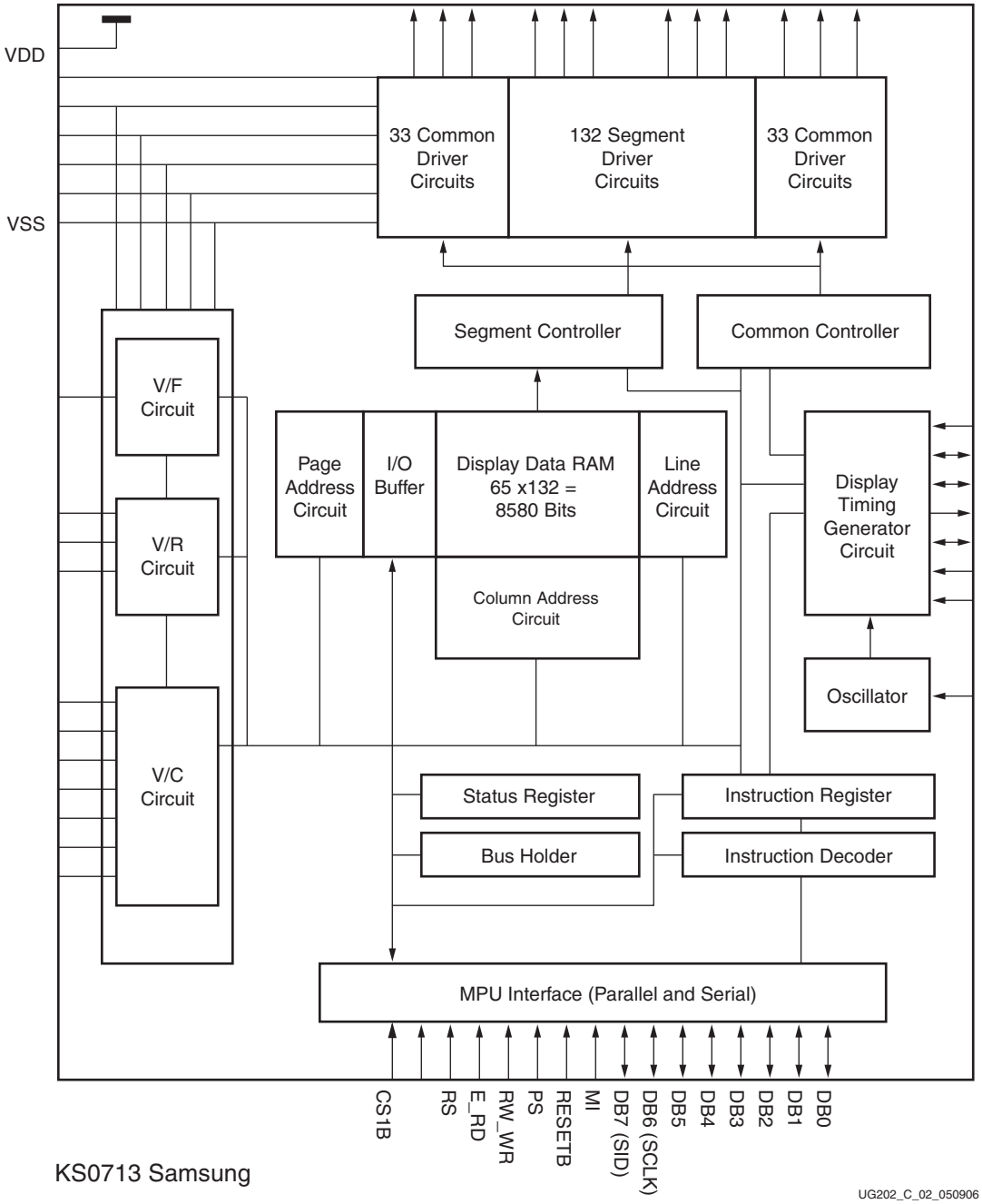

Figure C-2: **KS0713 Block Diagram**

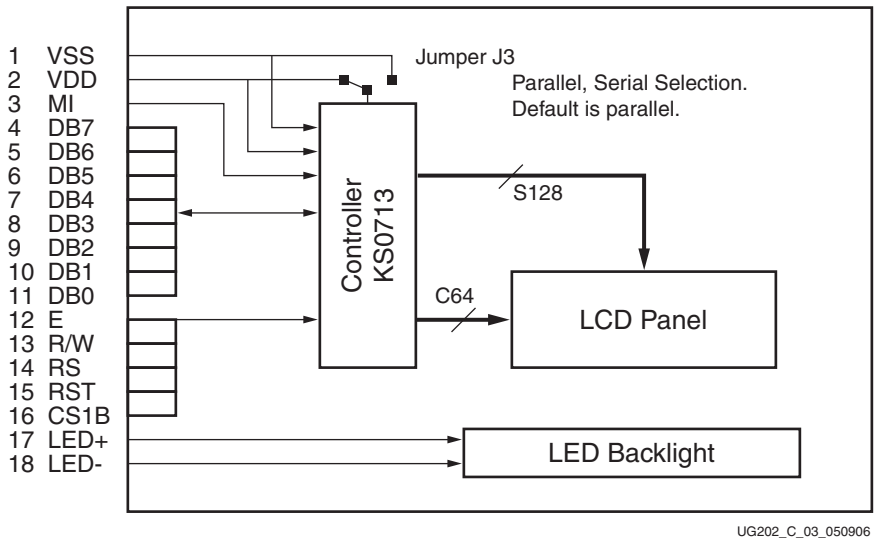

Figure C-3: **64128EFCBC-XLP Block Diagram**

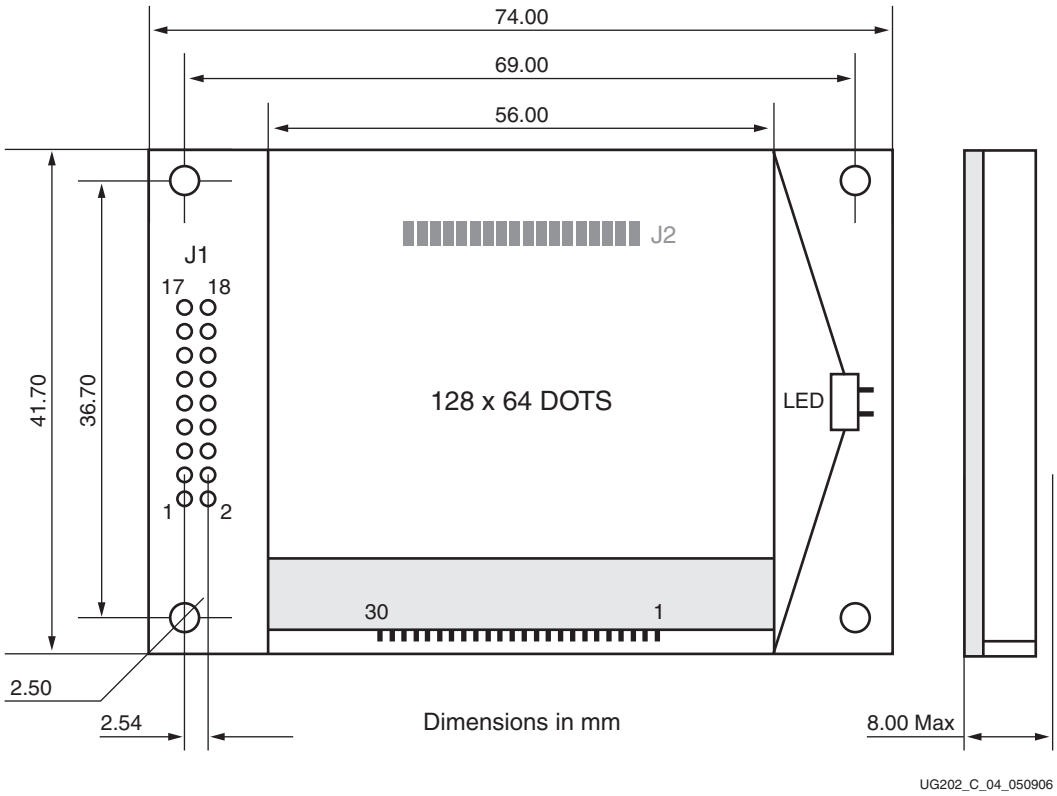

Figure C-4: **64128EFCBC-XLP Dimensions**

Controller – Operation

The pixels for the LCD panel are stored in the controller data RAM. This RAM is a 65-row by 132-column array. Each display pixel is represented by a single bit in the RAM array.

The interface to the RAM array goes through the 8-bit (DB0 – DB7) LCD interface. Therefore, the 65-bit rows are split into eight pages of eight lines. The ninth page is a single line page (DB0 only).

Interface designs can read from or write to the RAM array.

The display page is changed through the 4-bit page address register.

The column address (line address) is set with a two-byte register access. The line address corresponds to the first line that is going to be displayed on the LCD panel. This address is located in a 6-bit address register.

The RAM array is configured such that there are two characters per row (page), where each character pair uses eight rows of the display panel. Table C-2 shows the input data bytes, address lines, ADC control, and LCD outputs (segments).

Table C-2: **LCD Panel**

DB3	DB2	DB1	DB0	Data	Page	Line Address
0	0	0	0	DB0	Page 0	00H
				DB1		01H
				DB2		02H
				DB3		03H
				DB4		04H
				DB5		05H
				DB6		06H
				DB7		07H
0	0	0	1	DB0	Page 1	08H
				DB1		09H
				DB2		0AH
				DB3		0BH
				DB4		0CH
				DB5		0DH
				DB6		0EH
				DB7		0FH

Table C-2: **LCD Panel *(Continued)***

DB3	DB2	DB1	DB0	Data																			Line Address
0	0	1	0	DB0	■	■	■	■	■		■	■	■	■	■		Page 2							10H
				DB1	■						■													11H
				DB2	■						■													12H
				DB3	■	■	■	■			■	■	■	■										13H
				DB4	■						■													14H
				DB5	■						■													15H
				DB6	■	■	■	■	■		■													16H
				DB7																				17H
0	0	1	1	DB0		■	■	■			■				■		Page 3							18H
				DB1	■				■		■				■									19H
				DB2	■						■				■									1AH
				DB3	■		■	■	■		■	■	■	■	■									1BH
				DB4	■				■		■				■									1CH
				DB5	■				■		■				■									1DH
				DB6		■	■	■	■		■				■									1EH
				DB7																				1FH
0	1	0	0	DB0		■	■	■					■	■	■		Page 4							20H
				DB1			■							■										21H
				DB2			■							■										22H
				DB3			■							■										23H
				DB4			■							■										24H
				DB5			■				■			■										25H
				DB6		■	■	■				■	■											26H
				DB7																				27H
0	1	0	1	DB0	■				■		■						Page 5							28H
				DB1	■			■			■													29H
				DB2	■		■				■													2AH
				DB3	■	■					■													2BH
				DB4	■		■				■													2CH
				DB5	■			■			■													2DH
				DB6	■				■		■	■	■	■	■									2EH
				DB7																				2FH

Table C-2: **LCD Panel *(Continued)***

DB3	DB2	DB1	DB0	Data																				Line Address
0	1	1	0	DB0	■				■		■				■		Page 6							30H
				DB1	■	■		■	■		■				■									31H
				DB2	■		■		■		■	■			■									32H
				DB3	■		■		■		■		■		■									33H
				DB4	■				■		■			■	■									34H
				DB5	■				■		■				■									35H
				DB6	■				■		■				■									36H
				DB7																				37H
0	1	1	1	DB0		■	■	■			■	■	■	■			Page 7							38H
				DB1	■				■		■				■									39H
				DB2	■				■		■				■									3AH
				DB3	■				■		■	■	■	■										3BH
				DB4	■				■		■													3CH
				DB5	■				■		■													3DH
				DB6		■	■	■			■													3EH
				DB7																				3FH
1	0	0	0	DB0													Page 8							

Column Address																				
	ADC = 0	0	1	2	3	4	5	6	7	8	9	A	B		7E	7F	80	81	82	83
	ADC = 1	83	82	81	80	7F	7E	7D	7C	7B	7A	79	78		5	4	3	2	1	0
LCD Output		Seg 1	Seg 2	Seg 3	Seg 4	Seg 5	Seg 6	Seg 7	Seg 8	Seg 9	Seg 10	Seg 11	Seg 12		Seg 127	Seg 128	Seg 129	Seg 130	Seg 131	Seg 132

When a page is addressed, all the bits representing dots on the LCD panel can be accessed in that page. An array of 8x132 bits is available. The line address dictates what line of the RAM is going to be displayed on the first line of the glass panel.

Controller – LCD Panel Connections

The controller die, KS0713, connects to the LCD glass panel and user connection pins via a small PCB. Other necessary pins have default connections on the PCB. Table C-3 shows how all pins of the die are connected. The pins in blue connect to default values on the PCB, and the other pins connect to the user-accessible connectors.

Table C-3: **KS0713 Pin Connections**

Connector J1	Connector J2	PCB Connection	Connected to	Signal Name	Description
16	16	1		CS1B	Chip enable is active Low
15	15	2		RESETB	Initialize the LCD
14	14	3		RS	Register select
13	13	4		RW_WR	Read/Write
12	12	5		E_RD	Enable/Read
11	11	6		DB0	8-bit bidirectional data bus. In serial mode DB0-DB5 are High impedance, DB6 is the serial clock input, and DB7 is the serial data input.
10	10	7		DB1	
9	9	8		DB2	
8	8	9		DB3	
7	7	10		DB4	
6	6	11		DB5	
5	5	12		DB6	
4	4	13		DB7	
3	3	14		MI	Processor mode select
		15		PS	Parallel or Serial
1	1	16		VSS	Ground
2	2	17		VDD	Power Supply
LCD Control Pins					
			VDD	CS2	Active High chip enable.
			VDD	DUTY0	LCD driver duty ratio. Set to 1/65
			VDD	DUTY1	
			VDD	MS	Master / Slave operation. Set to Master
			VDD	CLS	Built-in oscillator enable
			VSS	TEMPS	Set to -0.05%/°C
			VDD	INTRS	Internal resistors used
			VSS	HPM	Normal mode set
			VDD	BSTS	Voltage converter input is VDD (2.4<VDD<3.6)

Table C-3: **KS0713 Pin Connections *(Continued)***

Connector J1	Connector J2	PCB Connection	Connected to	Signal Name	Description
			OPEN	DISP	Only used in Master/Slave
			OPEN	CL	Display clock input
			OPEN	M	Only used in Master/Slave
			OPEN	FRS	Only used in Master/Slave
Voltage Converter and Control					
		18		VOUT	Voltage converter in or out
		19		C3+	Voltage pump capacitors
		20		C3-	
		21		C1+	
		22		C1-	
		23		C2+	
		24		C2-	
		25		V0	LCD driver supply. The relationship of the voltages is V0>V1>V2>V3>V4>VSS. When the internal power supply is active, these voltages are generated.
		26		V1	
		27		V2	
		28		V3	
		29		V4	
		30		VSS1	
			VSS	DCDC5B	Power Supply Control
			OPEN	VR	V0 Adjustment pin

Controller – Power Supply Circuits

Figure C-5 shows the power supply circuits. The power supply is used in the five times boost mode, where VDD is 3.3V and VOUT is 16.5V. VOUT is the operating voltage of the operational amplifier delivering the operating voltage, V0, for the LCD panel.

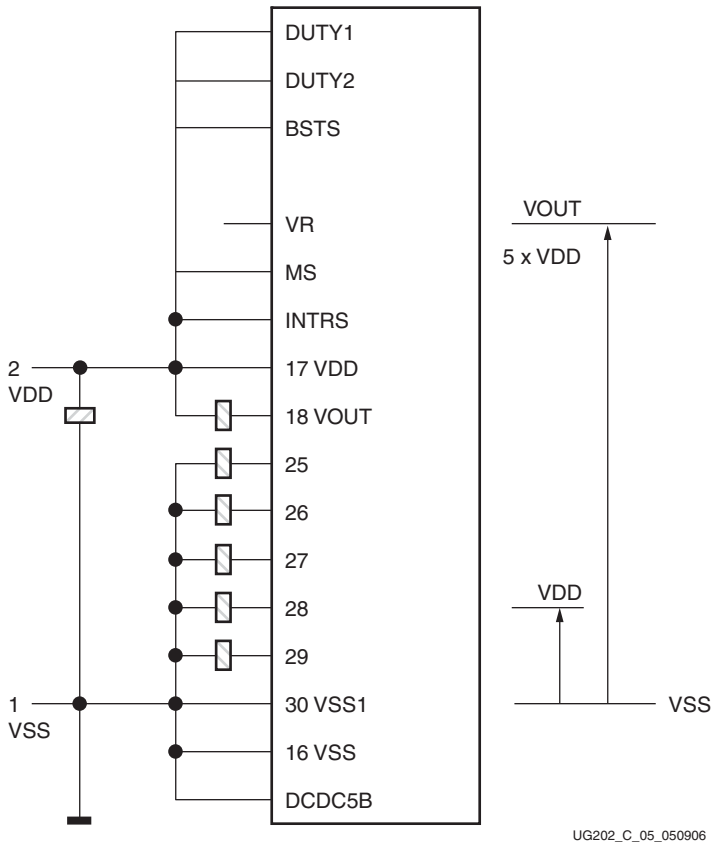

Figure C-5: **Power Supply Circuits**

The LCD operating voltage, V0, is set with two resistors, R_A and R_B. INTRS is driven Low when the resistors are external. INTRS is driven High when the resistors are internal. For the XlvdsPro_PwrIo board, internal resistors are selected.

The LCD operating voltage (V0) and the Electronic Volume Voltage (V_{EV}) can be calculated in units of V with these formulae:

$$V0 = \left(1 + \frac{R_B}{R_A}\right) \times V_{EV} \qquad \textit{Equation C-1}$$

$$V_{EV} = \left(1 - \frac{63 - \alpha}{300}\right) \times V_{REF} \qquad \textit{Equation C-2}$$

In Equation C-2, V_{REF} is equal to 2.0V at 25 °C.

The values of the reference voltage parameter, α, and the ratio R_A/R_B are determined with bit settings in the LCD controller's instruction registers. Thus, it is possible to change physical operating parameters of the LCD through register bit settings, controlling the operating voltage, and the electronic volume level.

The voltage and contrast settings must be configured before the LCD panel is ready for operation. Figure C-6 shows the initialization procedure required to set up the LCD controller.

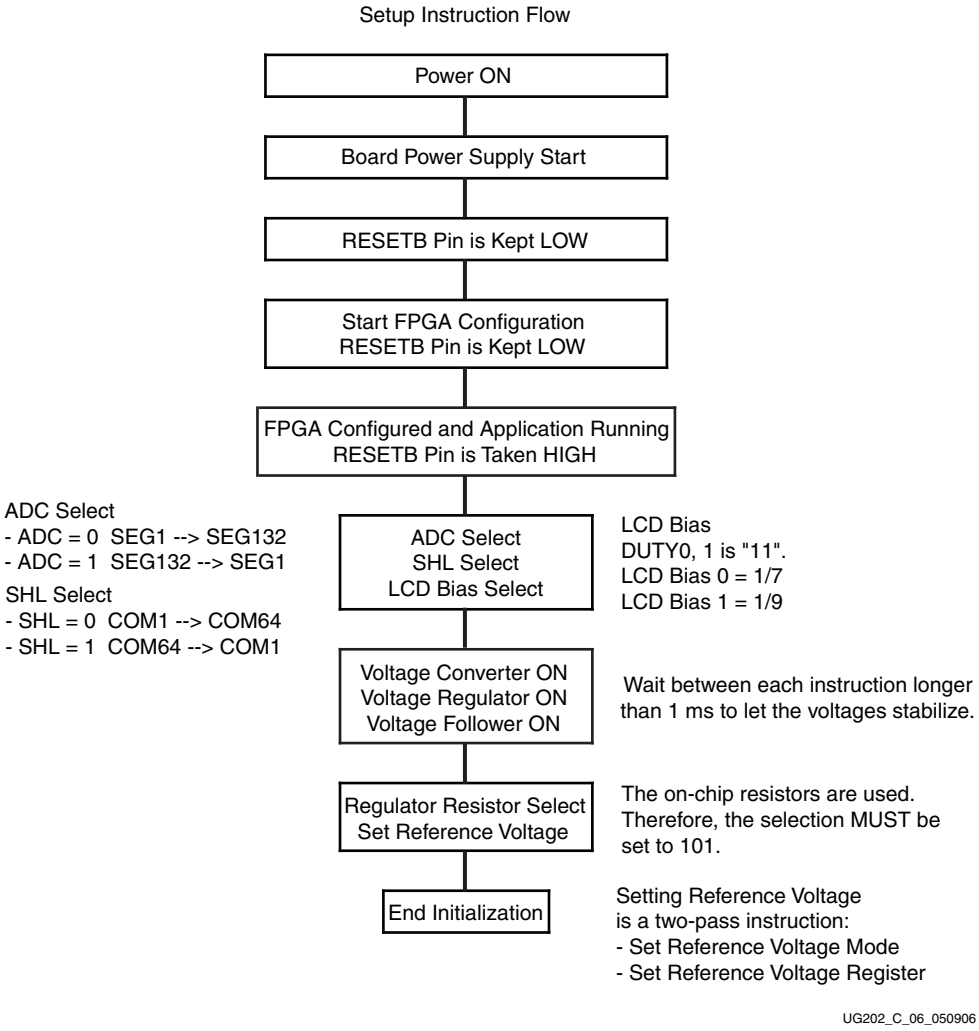

Figure C-6: **LCD Controller Initialization Flow**

Operation Example of the 64128EFCBC-3LP

The KS0713 LCD controller has several default settings of operation on the LCD panel display PCB. Some settings are forced through direct bonding on the chip. The default settings are:

- Master mode
- Parallel mode
- Internal oscillator
- Duty cycle ratio is set to 1/65
- Voltage converter input is between 2.4V ≤VDD ≤3.6V, where VDD connects to 3.3V
- Internal voltage divider resistors
- Temperature coefficient is set to -0.05%/°C

- Normal power mode is set
- The voltage follower and voltage regulator are set to:
  - Five times boost mode
  - The V4, V3, V2, V1, and V0 outputs depend on the bias settings of 1/9 or 1/7.

Because of these default settings, the following display controller connections are not used:

- DISP: Turns into an output when Master mode is selected
- FRS: Static driver segment output
- M: Used in Master/Slave display configurations
- CL: Clock pin used in Master/Slave display configurations

When RESETB is Low, the display controller is initialized as indicated in Table C-4.

Table C-4: **Display Controller Initialization (RESETB is Low)**

Parameter	Initial Value
Display	OFF
Entire display	OFF
ADC select	OFF
Reverse display	OFF
Power control	0,0,0 (VC, VR, VF)
LCD bias	1/7
Read-modify-write	OFF
SHL select	OFF
Static indicator mode	OFF
Static indicator register	0,0 (S1, S0)
Display start	0 (First line)
Column address	0
Page address	0
Regulator select	0,0,0 (R2, R1, R0)
Reference voltage	OFF
Reference Voltage register	1,0,0,0,0,0 (SV5, SV4, SV3, SV2, SV1, SV0)

When RESETB is High, the display must be initialized. The first steps to be taken to guarantee correct operation of the display and the controller are:

- Configure the ADC bit. This bit determines the scanning direction of the segments.
  - When the RESETB signal is active, ADC is reset to *0*, meaning that the segments are scanned from SEG1 up to SEG132.
  - When ADC is set to *1*, the segments are scanned in opposite direction.
- Configure the SHL bit. This bit sets the scanning direction of the COM lines.
  - When the RESETB signal is active, SHL is reset to *0*, meaning that the segments are scanned from COM1 up to COM64.

- When SHL is set to *1*, the common lines are scanned in opposite direction.

Once configured, these settings normally are not changed.

- Select the LCD bias settings.
  - The duty cycle is selected as 1/65 by hardwiring the controller IC pads on the display PCB.
  - The LCD bias is set to:
    - 1/7: when the BIAS bit is 0
    - 1/9: when the BIAS bit is 1

The following steps are performed next:

- Start the onboard converter, regulator, and follower
- Set the Regulator Resistor values (see Table C-5)
- Configure the reference voltage register parameters (see Table C-6)

Table C-5: **Resistor Value Settings**

	3-Bit Data Settings (R2 R1 R0)							
	000	001	010	011	100	**101**	110	111
1+(Rb/Ra)	1.90	2.19	2.55	3.02	3.61	**4.35**	5.29	6.48

Table C-6: **Reference Voltage Parameters**

SV5	SV4	SV3	SV2	SV1	SV0	Reference Voltage Parameter (α)
0	0	0	0	0	0	0
0	0	0	0	0	1	1
.. ..	.. ..	… ..	.. ..	.. ..	.. ..	.. ..
1	1	1	1	1	0	62
1	1	1	1	1	1	63

At startup of the LCD controller (after RESETB operation), the resistor and reference voltage values are:

- Resistor selection is: 0,0,0
- Reference voltage is: 1,0,0,0,0,0

The Resistor selection value MUST be set to 101b when using this LCD panel.

After the display is brought to operational mode, it is best to wait at least 1 ms to ensure the stabilization of power supply levels. After this time, all other necessary display initializations can be performed.

Instruction Set

Table C-7 shows the instruction set for the LCD panel.

Table C-7: **Display Instructions**

Instruction	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Read display data	1	1	Read Data							
8-bit data specified by the column and page address can be read from the Display Data RAM. The column address is increased automatically, thus data can be read continuously from the addressed page.										
Write display data	1	0	Write Data							
8-bit data can be written into a RAM location specified by the column and page address. The column address is increased automatically, thus data can be written continuously to the addressed page.										
Read status	0	1	BUSY	ADC	ONOFF	RESETB	0	0	0	0
BUSY: Device is BUSY when internal operation or reset. (0=active, 1 =busy). ADC: Indicates the relationship between RAM column address and segment driver. ONOFF: Indicates display ON or OFF status. RESETB: Indicates if initialization is in progress.										
Display ON/OFF	0	0	1	0	1	0	1	1	1	DON
Turn display ON or OFF. (1=ON, 0 = OFF)										
Initial display line	0	0	0	1	ST5	ST4	ST3	ST2	ST1	ST0

Sets the line address of the display RAM to determine the initial line of the LCD display.

ST5	ST4	ST3	ST2	ST1	ST0	
0	0	0	0	0	0	Line address 0
0	0	0	0	0	1	Line address 1
..	..	..	..	..	..	..
1	1	1	1	1	0	Line address 62
1	1	1	1	1	1	Line address 63

Set reference voltage mode	0	0	1	0	0	0	0	0	0	1
Set reference voltage register	0	0	x	x	SV5	SV4	SV3	SV2	SV1	SV0

This is a two-byte instruction. The first instruction sets the reference voltage mode. The second instruction sets the reference voltage parameter.

SV5	SV4	SV3	SV2	SV1	SV0	
0	0	0	0	0	0	0
0	0	0	0	0	1	1
..	..	..	..	..	..	..
1	1	1	1	1	0	62
1	1	1	1	1	1	63

Table C-7: **Display Instructions *(Continued)***

Instruction	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Set page address	0	0	1	0	1	1	P3	P2	P1	P0

This instruction sets the address of the display data page. Any RAM data bit can be accessed when its page address and column address are specified. Changing the Page Address does not affect the display status.

P3	P2	P1	P0	
0	0	0	0	page 0
0	0	0	1	page 1
..	..	..	..	…
0	1	1	1	page 7
1	0	0	0	page 8

Set column address MSB	0	0	0	0	0	1	Y7	Y6	Y5	Y4
Set column address LSB	0	0	0	0	0	0	Y3	Y2	Y1	Y0

This instruction sets the address of the display data RAM. When a read or write to or from the display data RAM occurs, the addresses are automatically increased.

Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0	
0	0	0	0	0	0	0	0	Col Addr 0
0	0	0	0	0	0	0	1	Col Addr 1
..	..	..	..	..	..	..	..	...
1	1	1	1	1	1	1	0	Col Addr 130
1	1	1	1	1	1	1	1	Col Addr 131

ADC select	0	0	1	0	1	0	0	0	0	ADC

This instruction changes the relationship between RAM column address and segment driver.

ADC = 0, SEG1 --> SEG132 default mode
ADC = 1, SEG132 --> SEG1

Table C-7: **Display Instructions *(Continued)***

Instruction	RS	RW	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
Reverse display ON/OFF	0	0	1	0	1	0	0	1	1	REV
<table><tr><td>REV</td><td>RAM bit data = '1'</td><td>RAM bit data = '0'</td></tr><tr><td>0</td><td>Pixel ON</td><td>Pixel OFF</td></tr><tr><td>1</td><td>Pixel OFF</td><td>Pixel ON</td></tr></table>										
Entire display ON/OFF	0	0	1	0	1	0	0	1	0	EON
This instruction forces the display to be turned on regardless of the contents of the display data RAM. The contents of the display data RAM are saved. This instruction has priority over reverse display.										
LCD bias select	0	0	1	0	1	0	0	0	1	BIAS
This instruction selects the LCD bias. <table><tr><td>Duty ratio</td><td>Bias = 0</td><td>Bias = 1</td></tr><tr><td>1/65</td><td>1/7</td><td>1/9</td></tr></table>										
Set modify-read	0	0	1	1	1	0	0	0	0	0
This instruction stops the automatic incrementing of the column address by a read operation. The automatic increment is still done with a write operation.										
Reset modify-read	0	0	1	1	1	0	1	1	1	0
This instruction resets the changed modify-read to the normal.										
Reset	0	0	1	1	1	0	0	0	1	0
This instruction resets the LCD controller registers to the default values. The instruction CANNOT initialize the LCD power supply initialized with RESETB.										
SHL select	0	0	1	1	0	0	SHL	x	x	x
This instruction sets the COM output scanning direction. SHL = 0, COM1 ----> COM64 (default) SHL = 1, COM64 ----> COM1										
Power Control	0	0	0	0	1	0	1	VC	VR	VF
This instruction selects one of the eight power circuit functions. In the case of the DisplayTech 64128EFCBC display, these must be kept at "000."										
Regulator resistor select	0	0	0	0	1	0	0	R2	R1	R0
This instruction selects the resistor ratio Rb/Ra.										
Set static indicator mode	0	0	1	0	1	0	1	1	0	SM
Set static indicator register	0	0	x	x	x	x	x	x	S1	S0
This is a two-byte instruction. The first instruction enables the second instruction. The second instruction update the contents of the static indicator register.										

Read/Write Characteristics (6800 Mode)

Table C-8: **Read/Write Characteristics in 6800 Mode**

Parameter	Signal	Symbol	Min	Typ	Max	Unit
Address setup time	RS	T_{AS}	13	-	-	ns
Address hold time		T_{AH}	17	-	-	ns
Data setup time	DB7 to DB0	T_{DS}	35	-	-	ns
Data hold time		T_{DH}	13	-	-	ns
Access time		T_{ACC}	-	-	125	ns
Output disable time		T_{OD}	10	-	90	ns
System cycle time	RS	T_{CYC}	400	-	-	ns
Enable pulse width	Read/write	E_RD	T_{PWR}	125	-	ns
			T_{PWW}	55	-	ns

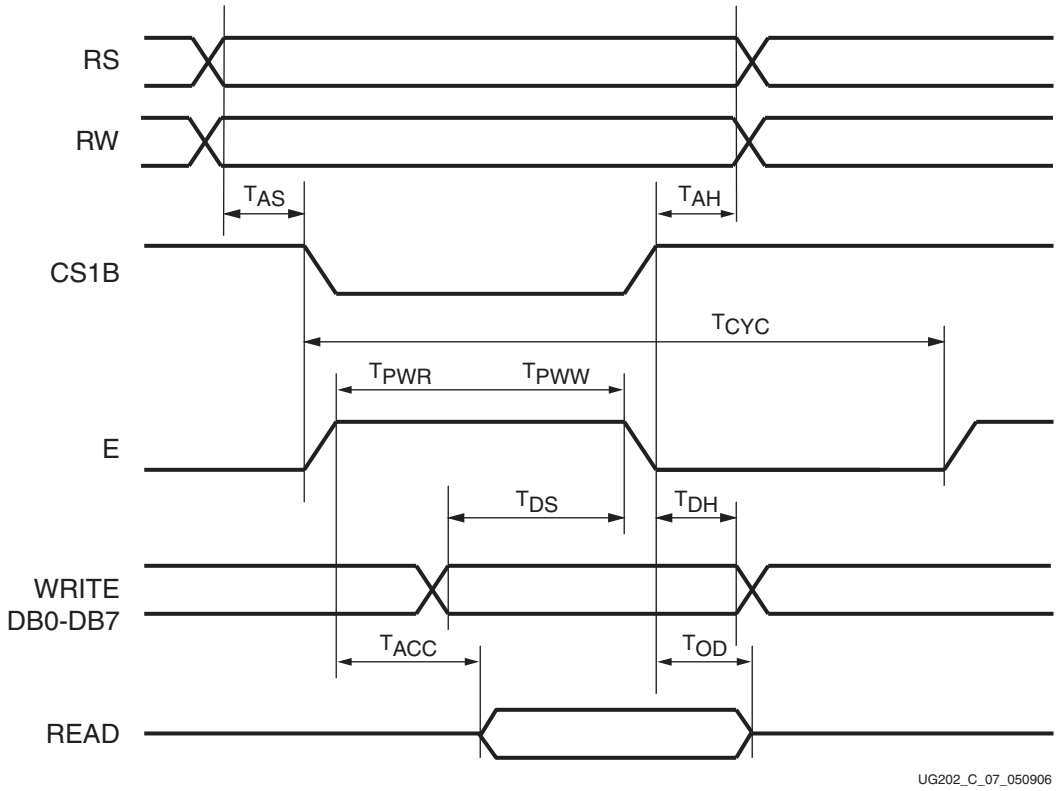

Figure C-7: **Read/Write Timing Waveforms (6800 Mode)**

Design Examples

LCD Panel Used in Full Graphics Mode

The LCD controller RAM has eight 132-byte pages (in fact, there are nine pages; page 9 is special). Each page is one-byte wide. If all the pages are put in one memory block, then the needed space is 8 pages x 8 bits x 132 pixels or 8448 bits (1056 bytes).

One Virtex-4 block RAM can be configured as 8+1 by 2048.

One block RAM can be used to store one complete pixel view of the LCD panel. There is enough space left for commands.

The ninth bit in the block RAM memory indicates whether the data in the block RAM is real data to be displayed or is a command for the controller.

The interface to the LCD panel is slow. The E signal can be used as the controller clock signal. This signal has a minimum cycle time of 400 ns for displaying 8 bits (equal to 8 dots) on the LCD. One full page of the display takes up to 132 x 400 ns = 52.8 µs. Updating the full display takes 52.8 µs x 8 = 423 µs.

If using the dual port and data width capabilities of the block RAM, writes to the block RAM can be 32 bits (+4 control bits), and reads from the block RAM on the LCD side can be 8 bits (1 control bit). An entire LCD page is updated in 33 write operations.

The interface on the LCD panel side sequentially reads the block RAM and thus updates the screen contiguously (like a television screen). The controller (microcontroller or other) side of the block RAM can be written at any time.

The write operation happens on the rising edge of the clock, and the read (LCD update) happens on the falling edge of the clock. Normally, write and read operations at the same address give corrupt read data when the read and write clock edges do not respect the clock-to-clock setup timing. This problem is solved by using both edges of the clock.

A state machine is used to provide correct timing of the signals on the LCD panel side. The panel can be used in write-only mode or in read/write mode. Most of the time LCD panels operate in write-only mode.

At first the block RAM must be initialized with some data (instructions to the LCD) to make the LCD operate correctly.

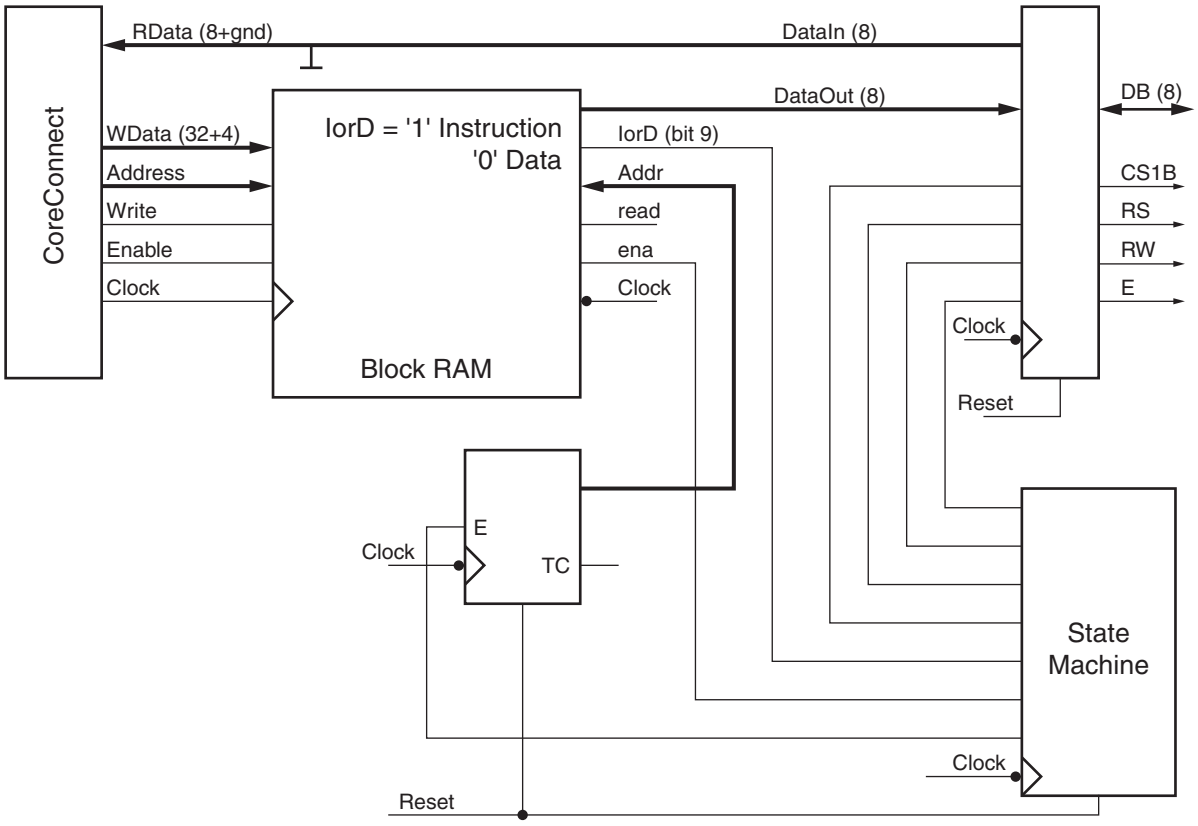

Figure C-8: **General Block Diagram of Panel in Full Graphics Mode**

LCD Panel Used in Character Mode

This design example requires a byte representing a command or data to be displayed as input.

- When the Enable signal is Low, nothing happens. The display interface design is locked.
- When the Enable signal is High and the “data_or_command” control signal is Low, the byte written is a display command.
- When the Enable signal and the data_or_command control signal are High, the byte written is the ASCII character code of the character to be put on the display.

Display Command Byte

The command set of the display can be found in Table C-7.

When the LCD interface is enabled for the first time, a set of command bytes is sent to the LCD. This command set provides the basic initialization of the LCD display controller. When this initialization is done, the normal LCD display interface is freed for normal use. Command bytes from the valid command set can be sent to the display (controller).

A detailed description of the LCD controller interface can be found in the `Toplevel.vhd.txt` file.

Display Data Byte

The supplied byte must be a valid ASCII representation of a character as shown in Figure C-9.

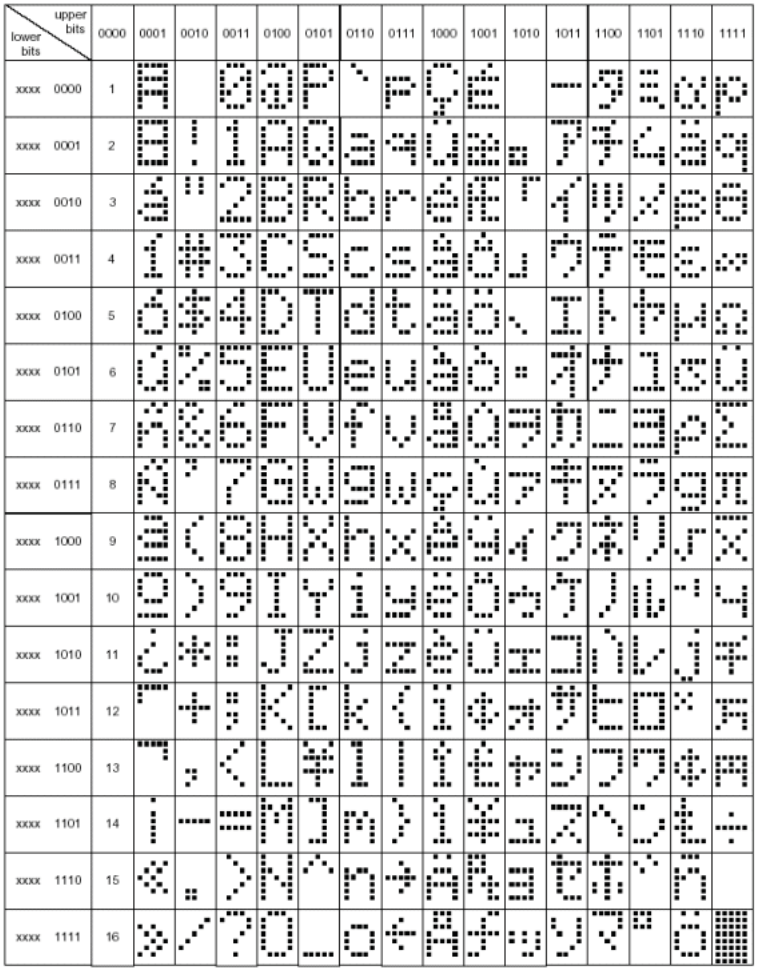

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Figure C-9: **ASCII Character Representations**

The character set is stored in block RAM (used as ROM). For the layout of the block RAM character set, see the `CharacterSet.xls` file. The block RAM (see Figure C-10) is organized as small arrays of eight bytes, which is easy for address calculation.

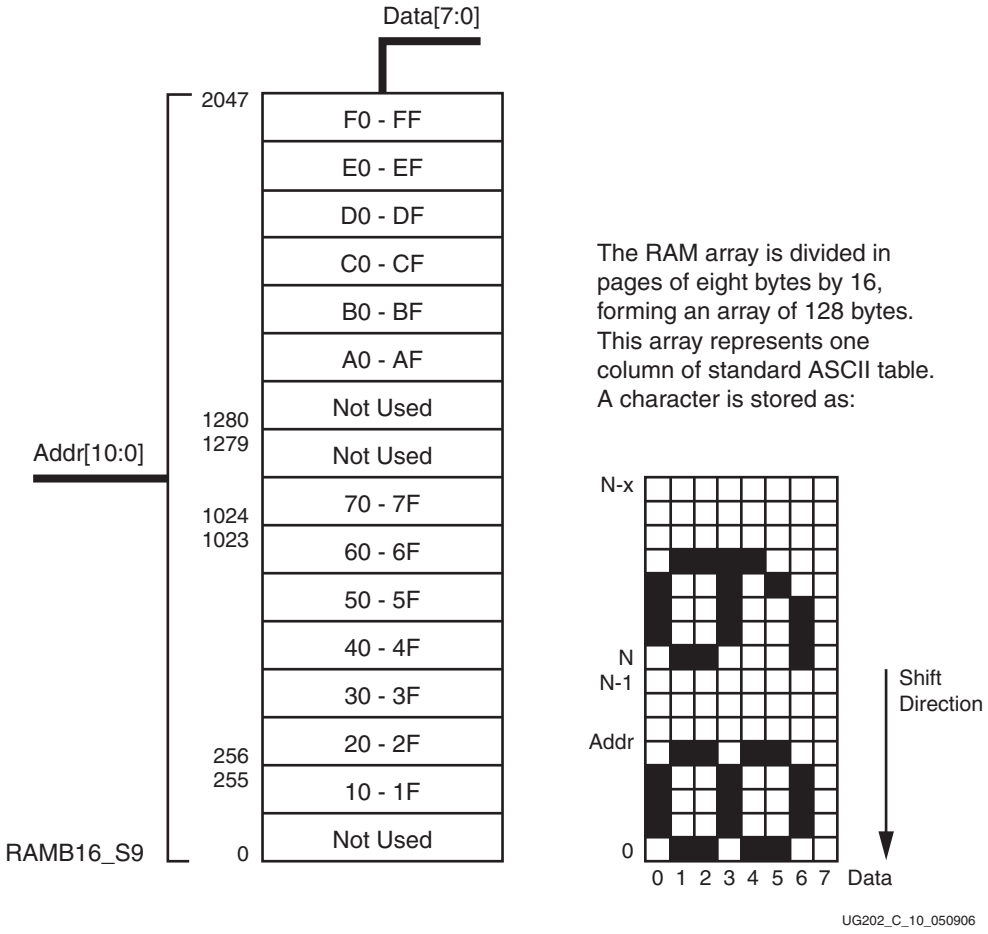


Figure C-10: **Block RAM Organization**

When presenting byte value 30 hex, character *0* must be displayed. Shifting the value 00110000b (30h) up three positions gives the value 180h or 348d.

Because each character uses eight byte locations, character *0* in the character set starts from memory location 348 decimal.

For example, character *X* has byte value 58h or 01011000b. Shifting this value three positions gives the value 2C0h or 704d.

Figure C-11 shows a block diagram of the LCD character generator controller. Character data is latched and then shifted left three positions. This shifted value is the start byte for a counter that outputs an address to the block RAM. The result is a stream of bytes representing a character for the display.

A small second counter determines when a new character is loaded into the block RAM address counter.

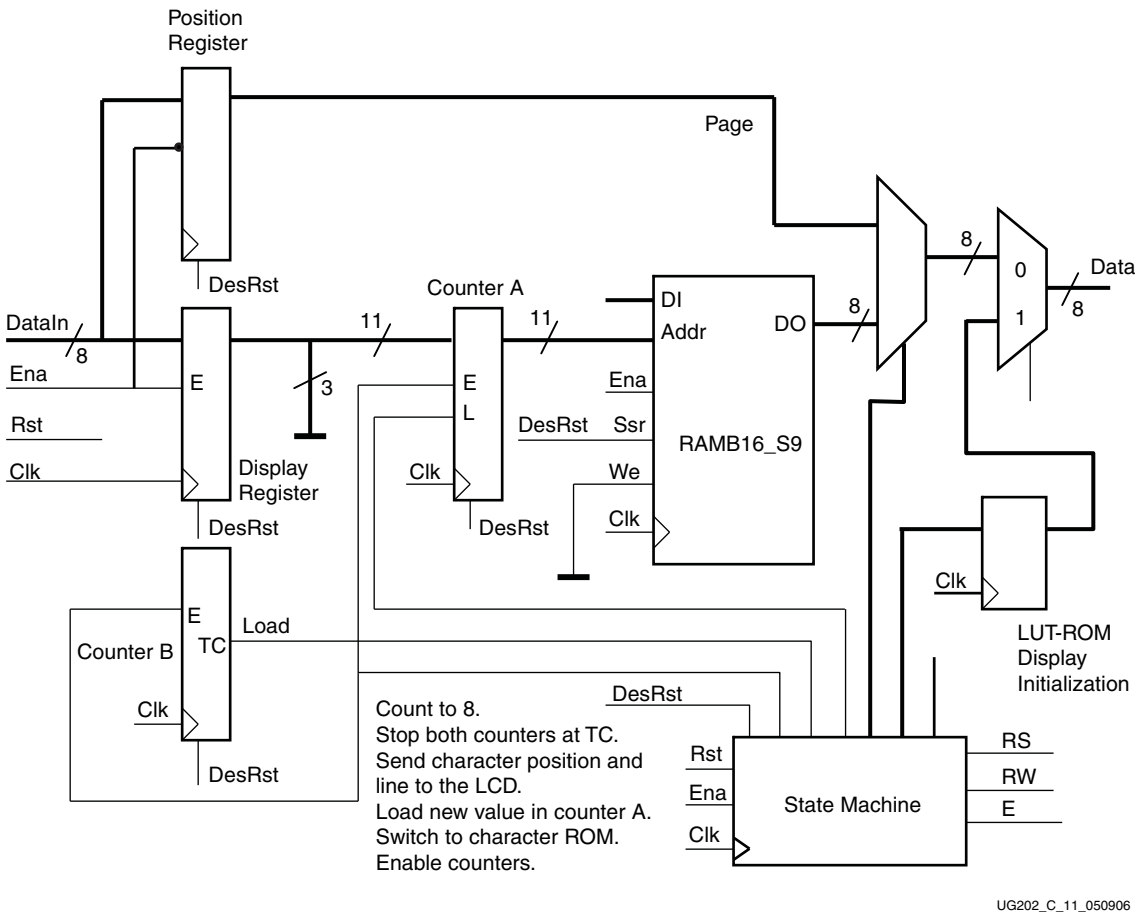


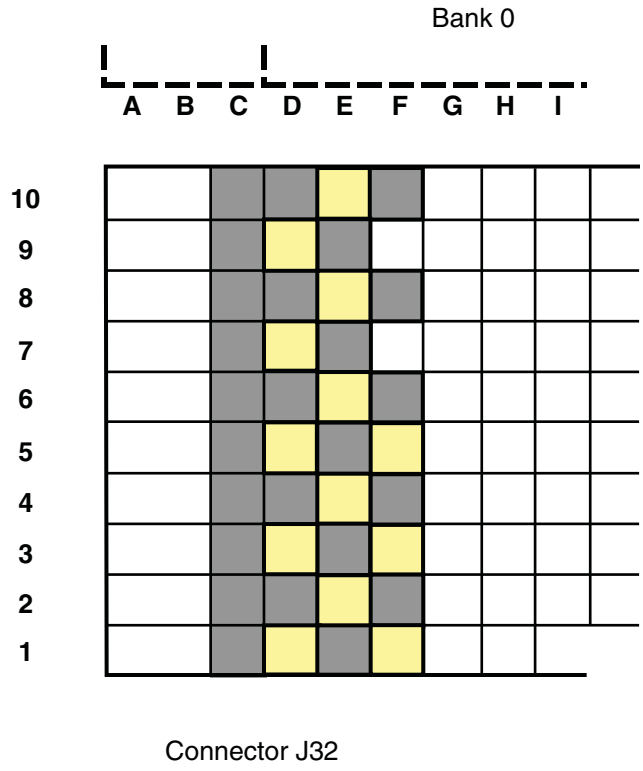
Figure C-11: **LCD Character Generator Controller**

A state machine takes care of the processing order.

A minimum cycle time of 400 ns on the E signal used as a reference. The 200 MHz system clock frequency is used as reference system clock. One E cycle uses at least 80 system clock cycles when the design is running at 200 MHz. The E pulse is part of the state machine, and the design only depends on the system clock. Timing is met as long as the system clock does not exceed 200 MHz.

This design can be adapted easily to fit the MicroBlaze™ or PPC405 CoreConnect bus system.

Array Connector Numbering



Connector Pin		FPGA Pin
D9	LCD_D0	G23
D7	LCD_D4	E22
D5	LCD_D5	E23
D3	LCD_D6	F23
D1	LCD_D7	F24
E10	LCD_RST	D24
E8	LCD_D1	F21
E6	LCD_D2	F22
E4	LCD_D3	G22
E2	LCD_ENA	H22
F5	LCD_R/W	G21
F3	LCD_RSEL	H21
F1	LCD_CS1B	C24

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Figure C-12: **LCD Connections (Bank 0)**

UCF Information

```
#
# Bank 0 / LCD-BUS
#
# NET "     " LOC ="F24 ";    # LCD_D7                IO0L02N
# NET "     " LOC ="F23 ";    # LCD_D6                IO0L02P
# NET "     " LOC ="E23 ";    # LCD_D5                IO0L03N
# NET "     " LOC ="E22 ";    # LCD_D4                IO0L03P
# NET "     " LOC ="G22 ";    # LCD_D3                IO0L06P
# NET "     " LOC ="F22 ";    # LCD_D2                IO0L07N
# NET "     " LOC ="F21 ";    # LCD_D1                IO0L07P
# NET "     " LOC ="G23 ";    # LCD_D0                IO0L05
# NET "     " LOC ="D24 ";    # LCD_RST               IO0L08N
# NET "     " LOC ="C24 ";    # LCD_CS1B              IO0L08P
# NET "     " LOC ="H21 ";    # LCD_RSEL              IO0L09N
# NET "     " LOC ="G21 ";    # LCD_RW                IO0L09P
# NET "     " LOC ="H22 ";    # LCD_ENA               IO0L06N
#
```

Appendix D

ML550 Starter UCF

UCF Starter File

The ML550 UCF starter file (`ml550_starter.ucf`) can be downloaded from the Xilinx website at: https://secure.xilinx.com/webreg/clickthrough.do?cid=37487.

Complete FPGA pinout information is included on the CD shipped with the Virtex-5 FPGA ML550 Networking Interfaces Platform kit.