# **inter<sub>sil</sub>**

## ISL95210 10A Integrated FET Regulator Evaluation Board Setup Procedure

This document describes the setup procedure for the ISL95210EVAL1Z Rev B board.

## Description

Increasing demand for circuit board real estate necessitates the use of a higher integration to reduce component count. To that end, Intersil introduces the ISL95210 regulator. It features integrated power MOSFET switches that are capable of delivering 10A continuous load current at elevated temperatures and maintaining high efficiency. Leveraging a highly digital feature set and the new R4<sup>TM</sup> modulator allows the ISL95210 to provide a fully regulated point of load solution with only four external components. For more information on the features of the ISL95210, see the data sheet  $\underline{FN6938}$ 

## What's Inside

The Evaluation Board Kit contains the following materials:

- ISL95210EVAL1Z REV B Board
- ISL95210 Data Sheet
- ISL95210 Evaluation Board Setup Procedure (this document)

## What's Needed

The following materials will be needed to perform testing:

- +5V, 10A Power Supply
- Precision Digital Multi-Meter
- Electronic Load
- 4-Channel Oscilloscope

NOTE: Amperage rating of power supplies are determined by maximum expected loading plus a percentage margin of error.

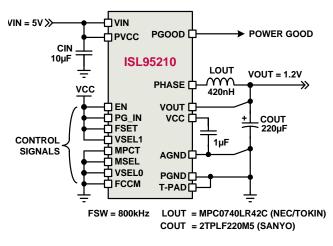


FIGURE 1. ISL95210 800kHz TYPICAL APPLICATION CIRCUIT

## **Quick Setup Guide**

- Step 1: Set the +5.0V power supply to +5V and place in the "STANDBY" or "OFF" position. Connect the positive terminal (+) of the supply to the +5V terminal TP4 and the negative terminal (-) of the supply to GND TP3.
- Step 2: Connect the positive terminal (+) of the electronic load to the V<sub>OUT</sub> terminal TP1. Connect the negative terminal (-) of the electronic load to the GND terminal TP2. Make sure the electronic load is set to the OA condition.
- Step 3: Check to ensure all jumpers and switches are in their default positions prior to application of power (refer to "Detailed Description of Switch Settings" and "Detailed Description of Jumper Settings" on page 2).
- Step 4: Set the power supply to the "ON" position. LED D1 should show Red. Check all power supply outputs with a DMM to ensure correct voltage levels. Adjust if necessary.
- Step 5: Move the ENABLE jumper to the "ON" position. LED D1 should show Green.
- Step 6: Measure V<sub>OUT</sub> with a DMM from TP5(+) to TP8(-). It should read 1.2V (±1%).

At this point, the board has been properly powered up. Normal testing can begin.

NOTE: If you need technical assistance, or other assistance, with the ISL95210 Evaluation Board, call 1-888-INTERSIL (468-3774).

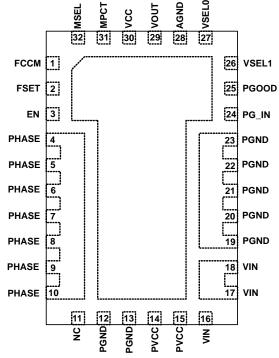


FIGURE 2. ISL95210 PINOUT 4x6mm 32 LD QFN (TOP VIEW)

#### **Detailed Description of Test Points**

TEST POINT	FUNCTION			
J1	V <sub>OUT</sub> Scope Probe Jack			
J2	PHASE Scope Probe Jack			
TP5	V <sub>OUT</sub>			
TP6	GND (V <sub>IN</sub> )			
TP7	V <sub>IN</sub>			
TP8	GND (V <sub>OUT</sub> )			
TP16	PG_IN (external source if J4 is OPEN)			
TP17	PGOOD			
TP18	+12V_AUX (if charge pump is disabled with J3)			

#### **Detailed Description of Switch Settings**

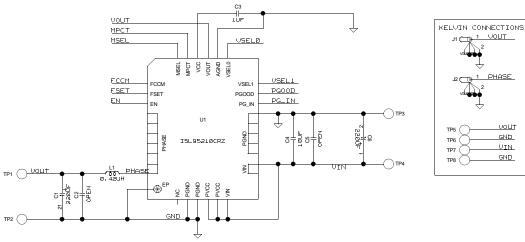
SWITCH	POSITION	FUNCTION	
S1	OFF	ENABLE On-Board Load Transient	

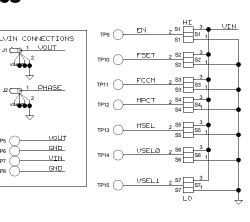
NOTE: The *POSITION* column reflects the default state of each switch or jumper.

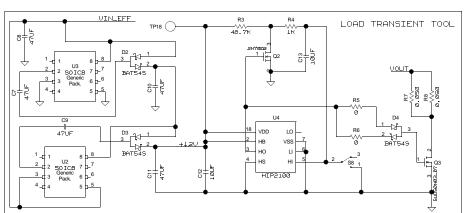
#### **Detailed Description of Jumper Settings**

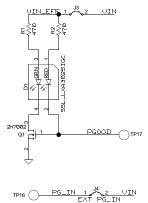
JUMPER	POSITION	FUNCTION						
S1	OFF	OFF = Regulator is disabled ON = Regulator is enabled						
S2	ON	OFF = 400kHz operation FLOAT = 533kHz operation ON = 800kHz operation						
S3	ON	OFF = Full DCM FLOAT = Ultra-sonic DCM ON = Full CCM						
S4	OFF	OFF = ±15% margin setpoint FLOAT = ±10% margin setpoint ON = ±20% margin setpoint						
S5	OFF	OFF = No margining FLOAT = Margin down ON = Margin up						
S6	OFF	OFF = VSELO logic low FLOAT = VSELO floating ON = VSELO logic high						
\$7	ON	OFF = VSEL1 logic low FLOAT = VSEL1 floating ON = VSEL1 logic high						
J3	CLOSED	CLOSED = LED and charge pump ON OPEN = LED and charge pump OFF						
J4	CLOSED	CLOSED = LED and charge pump ON OPEN = LED and charge pump OFF						

## **ISL95210EVAL1Z Evaluation Board Schematics**









## **Application Note 1485**

ITEM	QTY	REFERENCE	VALUE	TYPE	FOOTPRINT	VOLTAGE (V)
TOP LAYE	R					
1	1	C1	220µF	Sanyo-POSCAP 2TPLF220M5		2
2	1	СЗ	1µF	Generic MLCC X5R (or better)	0603	6.3
3	1	C4	10µF	Generic MLCC X5R (or better)	1206	6.3
4	1	L1	420nH	Tokin MPC0740LR42C	2525	
5	1	U1		ISL95210 10A Regulator	4x6mm QFN	
6	1	D1		Lumex SSL_LXA3025IGC LED	3x2 5mm	
7	1	<b>S</b> 8		C&K GT11MSCBE SPDT Switch		
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8	1	C2	DNP			
9	1	C5	DNP			
10	1	C6	330µF	Sanyo-POSCAP 6TPB330M		6.3
11	7	C7, C8, C9, C10, C11, C12, C13	10µF	Generic MLCC (X5R or better)	0805	16
12	2	R1, R2	470Ω	1% generic thick film chip resistor	0603	
13	1	R3	48.7kΩ			
14	1	R4	1kΩ			
15	2	R5, R6	249Ω			
16	1	R7	0.12Ω		2512	
17	1	R8	DNP			
18	3	D2, D3, D4		Generic BAT54S	S0T-23	
19	2	Q1, Q2		Generic 2N7002	S0T-23	
20	1	Q3		Vishay SUD50N03-07-E3	T0-252	
21	2	U2, U3		Intersil ICL7660 charge pump	SOIC8	
22	1	U4		Intersil HIP2100 half-bridge driver	SOIC8	

#### TABLE 1. BILL OF MATERIALS

NOTES:

1. Jumpers and test points not included in BOM as they represent non-critical components.

2. Components in **BOLD** represent the required components for a real application. The remainder are for board flexibility and evaluation.

## ISL95210EVAL1Z Layout

Board consists of 4 layers of 2 ounce copper

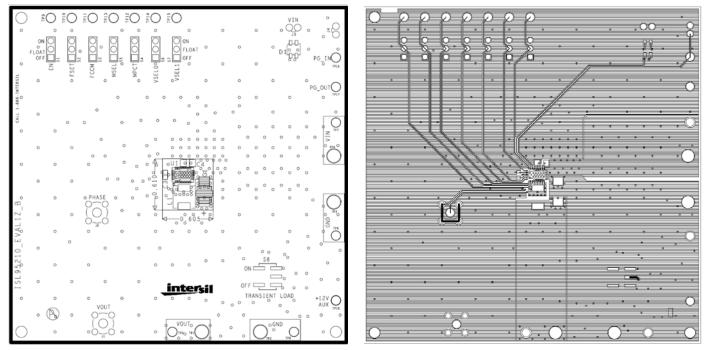


FIGURE 3. SILK SCREEN TOP

FIGURE 4. TOP LAYER

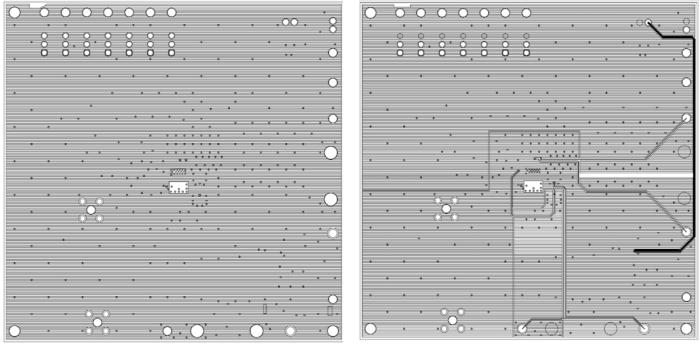


FIGURE 5. INTERNAL LAYER 1

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FIGURE 6. INTERNAL LAYER 2

## ISL95210EVAL1Z Layout (Continued)

Board consists of 4 layers of 2 ounce copper

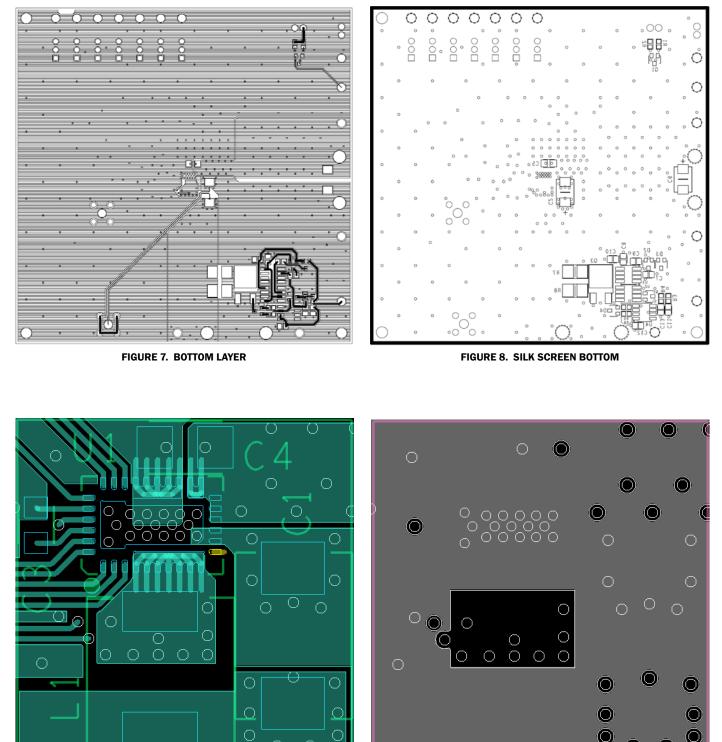


FIGURE 10. ZOOM OF APPLICATION ONLY (INTERNAL LAYER 1)

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## ISL95210EVAL1Z Layout (Continued)

Board consists of 4 layers of 2 ounce copper

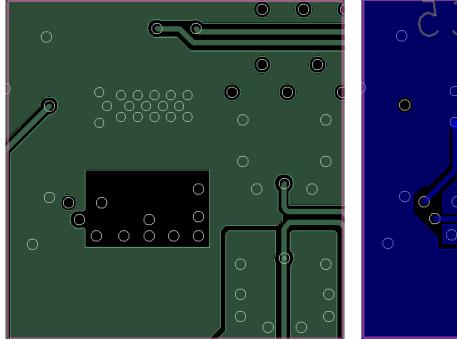


FIGURE 11. ZOOM OF APPLICATION ONLY (INTERNAL LAYER 2)

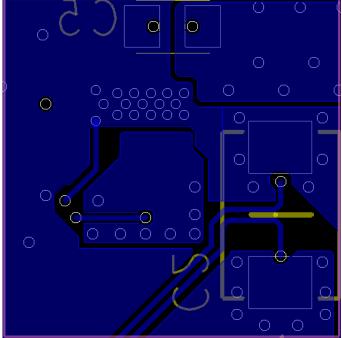


FIGURE 12. ZOOM OF APPLICATION ONLY (BOTTOM LAYER)

Intersil Corporation reserves the right to make changes in circuit design, software and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that the Application Note or Technical Brief is current before proceeding.

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