A111 – Pulsed Coherent Radar (PCR)

Datasheet v1.2

A111 Overview

The A111 is a radar system based on pulsed coherent radar (PCR) technology and is setting a new benchmark for power consumption and distance accuracy – fully integrated in a small package of 29 mm^2.

The A111 60 GHz radar system is optimized for high precision and ultra-low power, delivered as a one package solution with integrated Baseband, RF front-end and Antenna in Package (AiP). This will enable easy integration into any portable battery driven device.

The A111 is based on leading-edge patented sensor technology with pico-second time resolution, capable om measuring absolute distance with mm accuracy up to a range of 2 m [1] and with a continuous sweep update frequency fully configurable up to 1500 Hz [2].

The A111 60 GHz radar remains uncompromised by any natural source of interference, such as noise, dust, color and direct or indirect light.

Applications

- High precision distance measurements with mm accuracy and high update frequency
- Proximity detection with high accuracy and the possibility to define multiple proximity zones
- Motion detection, Speed detection
- Enables material detection
- High precision object tracking, enabling gesture control
- High precision tracking of 3D objects
- Monitor vital life signs such as breathing and pulse rate
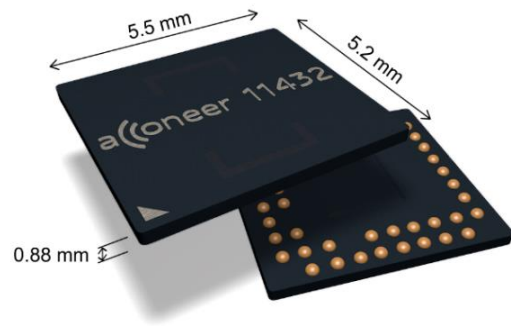
Features

- **Fully integrated sensor**
  - 60 GHz Pulsed Coherent Radar (PCR)
  - Integrated Baseband, RF front-end and Antenna in Package (AiP)
  - 5.5 x 5.2 x 0.88 mm fcCSP, 0.5 mm pitch
- **Accurate distance ranging and movements**
  - Measures absolute range up to 2 m [1]
    - Absolute accuracy in mm
  - Relative accuracy in µm
  - Possible to recognize movement and gestures for several objects
  - Support continuous and single sweep mode
  - Continuous sweep update rate up to 1500 Hz [2]
  - HPBW of 80 (H-plane) and 40 degrees (E-plane)
- **Easy integration**
  - One chip solution with integrated Baseband and RF
  - Can be integrated behind plastic or glass without any need for a physical aperture
  - Single reflowable component
  - 1.8 V single power supply, enable with Power in Reset (PoR)
  - Clock input for crystal or external reference clock, 20-80 MHz
  - SPI interface for data transfer, up to 50 MHz SPI clock support
  - INTERRUPT support

[1] *2m ranging is guaranteed for an object size, shape and dielectric properties corresponding to a spherical corner reflector of 5 cm radius.*
[2] *System integration dependent – e.g. Host MCU and SPI performance.*

Table of Contents

1 Revision History

| Revision	Comment
V1.0	Released version
V1.1	Minor reference correction in chapter 5.1. A111 marking info added in chapter 2.
V1.2	Relative phase accuracy added in chapter 6.3

2   Description

The A111 is an optimized low-power, high-precision, 60 GHz radar sensor with integrated Baseband, an RF front-end and an Antenna in Package (AIP).

The sensor is based on pulsed coherent radar (PCR) technology, featuring a leading-edge patented solution with picosecond time resolution. The A111 is the perfect choice for implementing high-accuracy, high-resolution sensing systems with low-power consumption.

Device Information

Part number	Package	Size (nom)
A111 R2	fcCSP, 50 pin	5.2 mm x 5.5 mm x 0.88 mm

Acconeer A111 marking
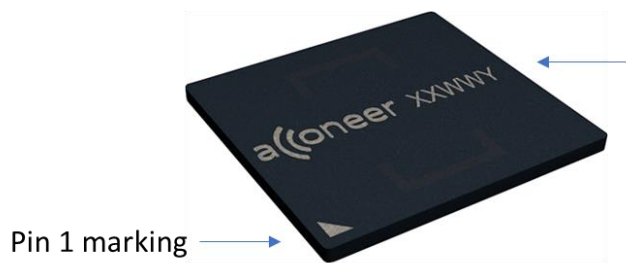
A111 marking:
- XX = Product code
- WW = Manufacturing week
- Y = Manufacturing year

Pin 1 marking

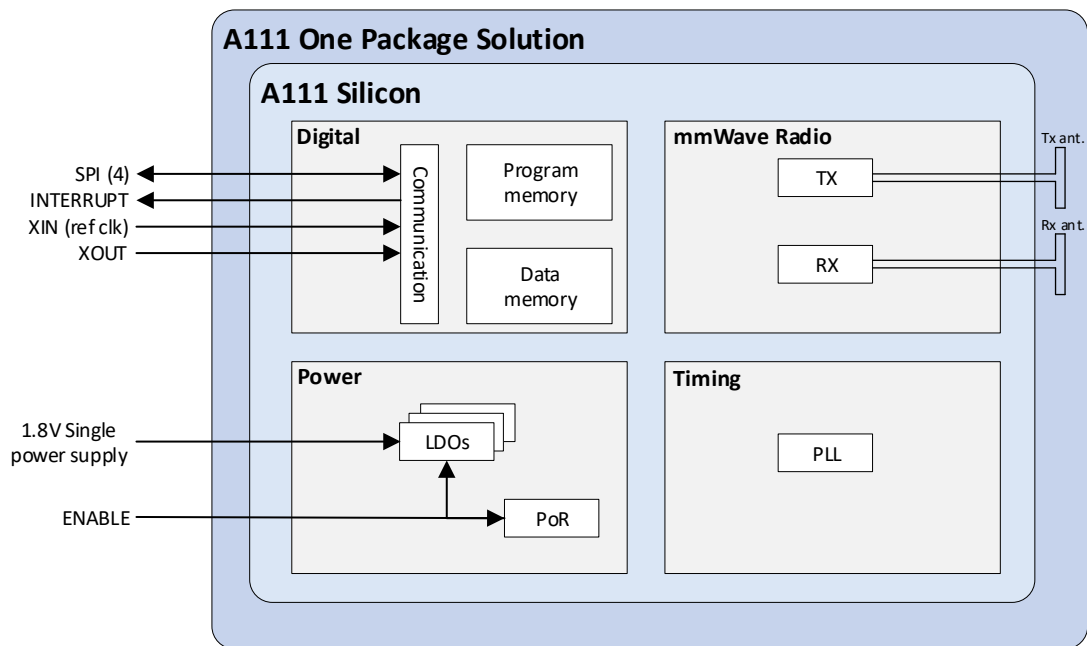2018-06-25

2.1 Functional Block Diagram

Figure 2.1. The A111 functional block diagram.

The A111 silicon is divided into four functional blocks: Power, Digital, Timing and mmWave radio.

The Power functional block includes LDOs and a Power on Reset (PoR) block. Each LDO creates its own voltage domain. The PoR block generates a Reset signal on each power-up cycle. The host interfaces the Power functional block of the sensor via 1.8V Single power supply and ENABLE.

The Digital functional block includes sensor control. The data memory stores the radar sweep data from the ADC. The host interfaces the Sensor via a 4 pin SPI interface, a Clock (XIN, XOUT) and INTERRUPT signal.

The Timing block includes the timing circuitry.

The mmWave radio functional block generates and receives radar pulses and includes transmitter (TX), receiver (RX) and interfaces toward the integrated antennas.

3 Pin Configuration and Functions

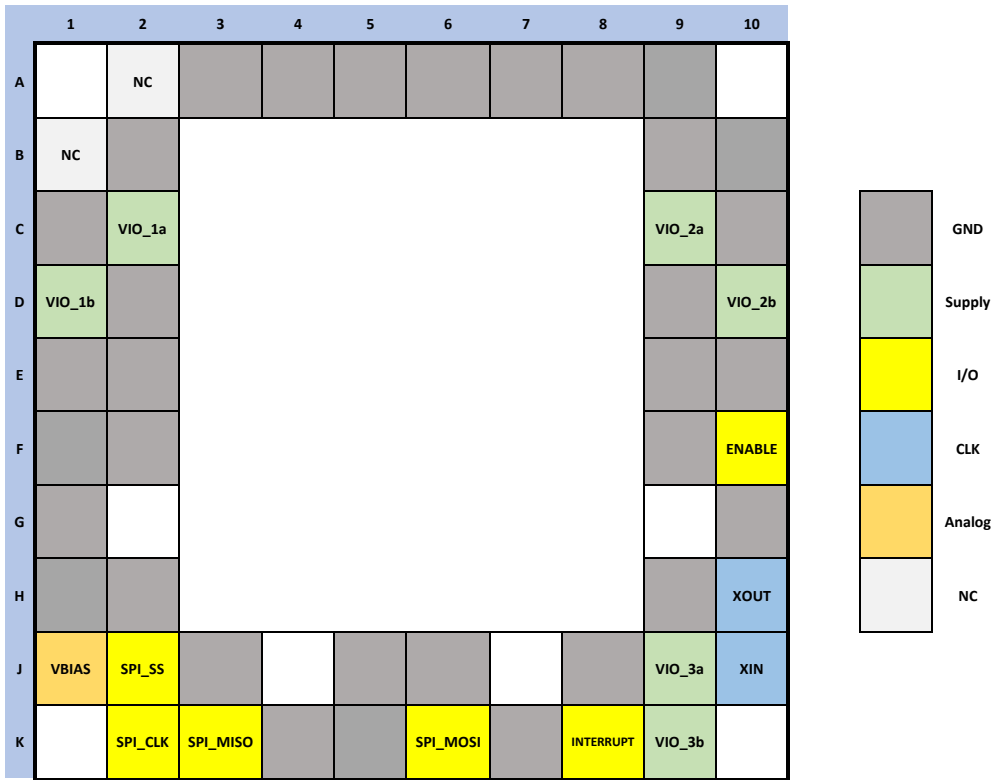The below figure shows the A111 pin configuration, top view:

Figure 3.1. Pin configuration of the A111 sensor, top view.

The below table shows the A111 total number of 50 pins:

Pin	Pin name	Pin type	Description	Comment
A2	NC		No connect	
A3-A8	GND	Ground	Must be connected to solid ground plane	
A9	GND	Ground	Must be connected to solid ground plane	
B1	NC		No connect	
B2, B9	GND	Ground	Must be connected to solid ground plane	
B10	GND	Ground	Must be connected to solid ground plane	
C1	GND	Ground	Must be connected to solid ground plane	
C2	VIO_1a	Supply voltage	Supply voltage, RF part [1]	
C9	VIO_2a	Supply voltage	Supply voltage, RF part [1]	
C10	GND	Ground	Must be connected to solid ground plane	
D1	VIO_1b	Supply voltage	Supply voltage, RF part [1]	
D2, D9	GND	Ground	Must be connected to solid ground plane	
D10	VIO_2b	Supply voltage	Supply voltage, RF part [1]	
E1, E2, E9, E10	GND	Ground	Must be connected to solid ground plane	
F1	GND	Ground	Must be connected to solid ground plane	

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Pin	Pin name	Pin type	Description	Comment
F2, F9	GND	Ground	Must be connected to solid ground plane	
F10	ENABLE	I/O	Must be connected to host MCU available GPIO. ENABLE is active high	
G1, G10	GND	Ground	Must be connected to solid ground plane	
H1	GND	Ground	Must be connected to solid ground plane	
H2, H9	GND	Ground	Must be connected to solid ground plane	
H10	XOUT	CLK	XTAL out	No connect if no XTAL
J1	VBIAS	Analog	The analog pin VBIAS must be connected to VIO_3	
J2	SPI_SS	I/O	SPI slave select, active low select.	
J3, J5, J6, J8	GND	Ground	Must be connected to solid ground plane	
J9	VIO_3a	Supply voltage	Supply voltage, digital part [1]	
J10	XIN	CLK	XTAL input OR external ref clk input	1.1V domain
K2	SPI_CLK	I/O	SPI Serial Clock	
K3	SPI_MISO	I/O	Master Input – Slave Output	
K4	GND	Ground	Must be connected to solid ground plane	
K5	GND	Ground	Must be connected to solid ground plane	
K6	SPI_MOSI	I/O	Master Output – Slave Input	
K7	GND	Ground	Must be connected to solid ground plane	
K8	INTERRUPT	I/O	Interrupt signal, always output, that can be used as an interrupt in the host, more details are found in section 7, *Description*.	
K9	VIO_3b	Supply voltage	Supply voltage, digital part [1]	

Table 3.1. A111 sensor pin list

(1) VIO_1a and VIO_1b are short circuit inside the sensor. VIO_2a and VIO_2b are short circuit inside the sensor. VIO_3a and VIO_3b are short circuit inside the sensor.

4 Specifications

4.1 Absolute Maximum Ratings

The below table shows the A111 absolute maximum ratings over operating temperature range, on package, unless otherwise noted:

Parameter	Description	Min.	Max.	Unit
VIO_1 [2]	1.8 V RF power supply	0	2.0	V
VIO_2 [2]	1.8 V RF power supply	0	2.0	V
VIO_3	1.8 V digital power supply	0	2.0	V
XIN [1]	Clock input port for crystal or reference clock	-0.5	1.6	V
I/O	I/O supply voltage	-0.5	VIO_3+0.5	V
T_{OP}	Operating temperature range	-40	85	°C
T_{STG}	High temperature storage		150	°C

Table 4.1. Absolute maximum ratings

(1) XIN input may not exceed 0V when ENABLE is low.
(2) VIO_1 and VIO_2 must never exceed VIO_3.

Stresses beyond those listed in table 4.1 may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions or at any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods of time may affect device reliability.

4.2 Environmental Sensitivity

The below table shows the A111 environmental sensitivity:

Parameter	Standard	Max.	Unit
Storage temperature	JESD22-A103 [1]	150[1]	ºC
Reflow soldering temperature [1]	J-STD-020 [1]	260	ºC
Moisture Sensitivity Level	JESD22-A113 [1]	MSL3	
ESD, Charge Device Model (CDM)	JS-002, Class C2	500	V
ESD, Human Body Model (HBM)	JS-001, Class 1C	1000	V
Latch-up	JESD78, Class I	Pass	

Table 4.2 Environmental sensitivity

(1) For reference only. The package is generically qualified by the manufacturer. Acconeer does not guarantee adherence to standard.

4.3 Recommended Operating Conditions

The below table shows the A111 recommended operating conditions, on package:

Parameter	Min.	Typ.	Max.	Unit
Operating power supply voltage, VIO_1	1.71	1.8	1.89	V
Operating power supply voltage, VIO_2	1.71	1.8	1.89	V
Operating power supply voltage VIO_3	1.71	1.8	1.89	V
I/O operating range	-0.3		VIO_3+0.3	V
XIN operating range [1]	-0.3		1.2	V
Operating temperature	-40		85	ºC

Table 4.3. Recommended operating conditions

(1) XIN input must not exceed 0V when ENABLE is low.

4.4 Electrical Specification

The below table shows the A111 electrical DC specification conditions, on package, at $T_A = 25ºC$:

Parameter	Min.	Typ.	Max.	Unit
Current into any power supply pin			100	mA
I/O V_{IL} Low-level input voltage	-0.3		0.10*VIO_3	V
I/O V_{IH} High-level input voltage	0.90*VIO_3		VIO_3+0.3	V
I/O V_{OL} Low-level output voltage			0.4	V
I/O V_{OH} High-level output voltage	1.6			V
I/O I_{OL} (VOL = 0.4V)		7.8		mA
I/O I_{OH} (VOH = VIO_3-0.4)		5.8		mA
I/O I_{IL} Low-level input current		<1		µA
I/O I_{IH} High-level input current		<1		µA
XIN V_{IL} Low-level input voltage	-0.3		0.4	V
XIN V_{IH} High-level input voltage	1.0		1.2	V
XIN I_{IL} Low-level input current		<1		µA
XIN I_{IH} High-level input current		<1		µA

Table 4.4. Electrical DC conditions

The below table shows the A111 electrical AC specification conditions, on package, at $T_A = 25°C$:

Parameter	Min.	Typ.	Max.	Unit
I/O output operating frequency			100	MHz
I/O load capacitance			20	pF
XIN operating frequency	20		80[1]	MHz
XIN pin capacitance		0.2		pF

Table 4.5 Electrical AC conditions

(1) The maximum external reference clock frequency is 80 MHz and the maximum XTAL frequency is 50 MHz.

4.5 Power Consumption Summary

The below table summarizes the power consumption, maximum current ratings and average current ratings at all power terminals (VIO_1, VIO_2, VIO_3), at $T_A = 25°C$, VIO 1.8 V:

Parameter	Min.	Typ.	Max.	Unit
Current consumption, continuous TX active mode		71		mA
Average power consumption, 0.1 Hz sweep rate [2]		0.2 [1]		mW
Average power consumption, 10 Hz sweep rate [2]		3 [1]		mW
Average power consumption, 100 Hz sweep rate		20 [1]		mW
Current leakage at ENABLE low		66		µA

Table 4.6. Maximum and Average current ratings at power terminals.

(1) Measuring window set to 0.24 m, configuration with maximize on depth resolution used. Leakage current in ENABLE low not removed.
(2) Supply voltage turned off in between measurements.

4.6 RF Specification

The below table shows the A111 RF specification:

Parameter	Min.	Typ.	Max.	Unit
Center frequency fc		60.5		GHz
EIRP		10		dBm
HPBW, elevation plane [1]		40		degrees
HPBW, horizontal plane [1]		80		degrees
Update frequency (configurable) [2]			1500	Hz

Table 4.7 A111 RF specification

(1) See chapter 6 Typical Characteristics for elevation (E-plane) and horizontal (H-plane) HPBW.
(2) System integration dependent e.g. Host MCU and SPI performance.

5 Timing Requirements

5.1 Serial Peripheral Interface

The Serial Peripheral Interface (SPI) is a 4-wire serial bus, used for configuration and reading output from the A111 radar sensor. The A111 radar sensor is an SPI slave device connected to the SPI master, as described in figure 5.1. The A111 allows several devices to be connected on the same SPI bus, with a dedicated slave-select signal. Daisy-chain is not supported.
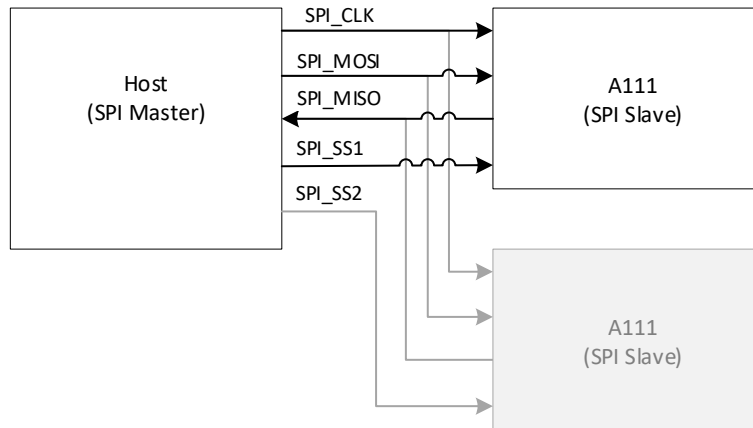

Figure 5.1. SPI master-slave connection

The serial data transfer input (MOSI) and output (MISO) to the A111 are synchronized by the SPI_CLK. The Slave Select signal (SS) must be low before and during transactions. The MOSI is always read on the rising edge of SCLK and the MISO changes value on the falling edge of SPI_CLK (SPI mode 0, CPOL/CPHA = 0). SS requires release in between transactions. See figure 5.2 and table 5.1 for timing characteristics.
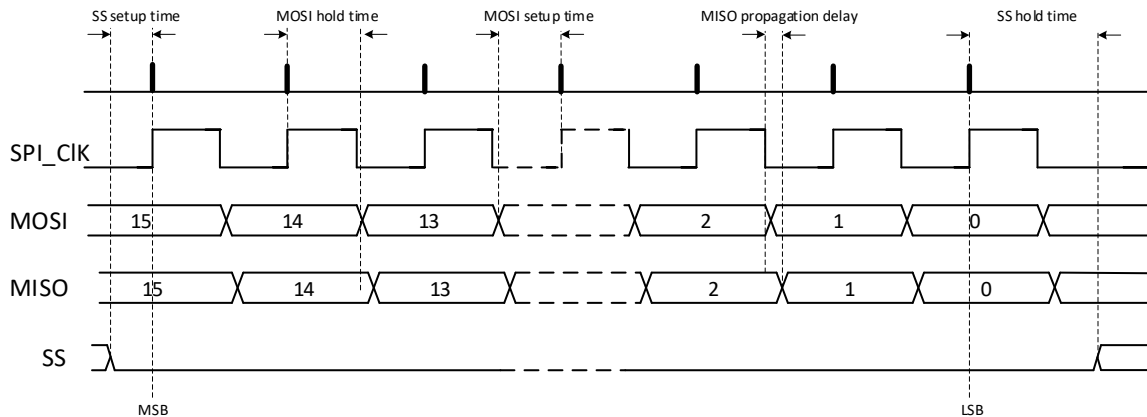

Figure 5.2: Timing diagram of SPI, CPOL=0 and CPHA=0.

Parameter	Min.	Typ.	Max.	Unit
Clock frequency [1]			50	MHz
SS setup time	1.0			ns
SS hold time	2.0			ns
MOSI setup time	1.0			ns
MOSI hold time	2.5			ns
MISO propagation delay [2]			5.5	ns

Table 5.1 SPI timing characteristics

(1) The 50 MHz clock frequency requires that the reference clock is at least 20.625 MHz

(2) 10pF load on SPI_MISO

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6   Typical Characteristics

6.1 Distance Accuracy

Conditions: T_A = 25 ℃, V_{DD} = 1.8 V. Statistical result based on sweep count 100, 20 tested devices.

The below figure shows the standard deviation of distance estimation, configuration with maximize on depth resolution used, 0.06-0.30 m. Object metal cylinder, 40 mm in diameter.
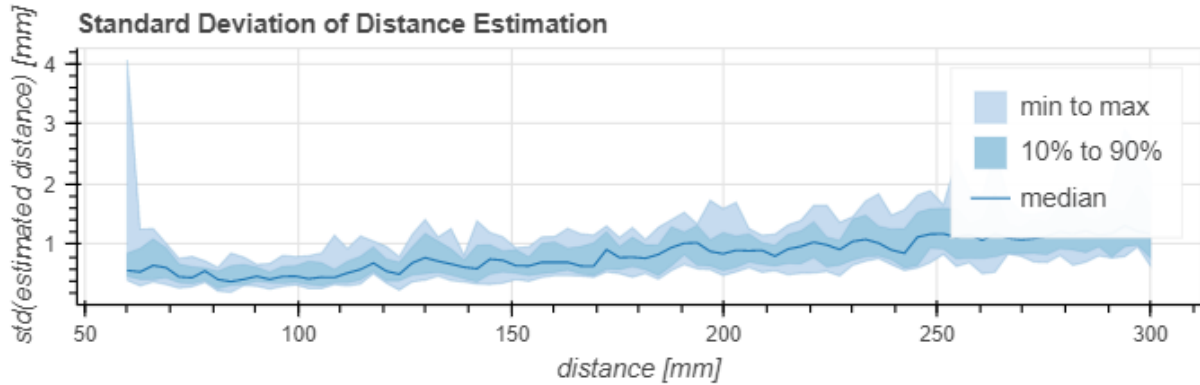
Figure 6.1. Standard deviation of distance estimation, maximize on depth resolution 0.06-0.30 m.

The below figure shows the standard deviation of distance estimation, configuration with maximize on SNR used, 1.76-2.0 m. Object 50 mm radius spherical metal corner reflector.
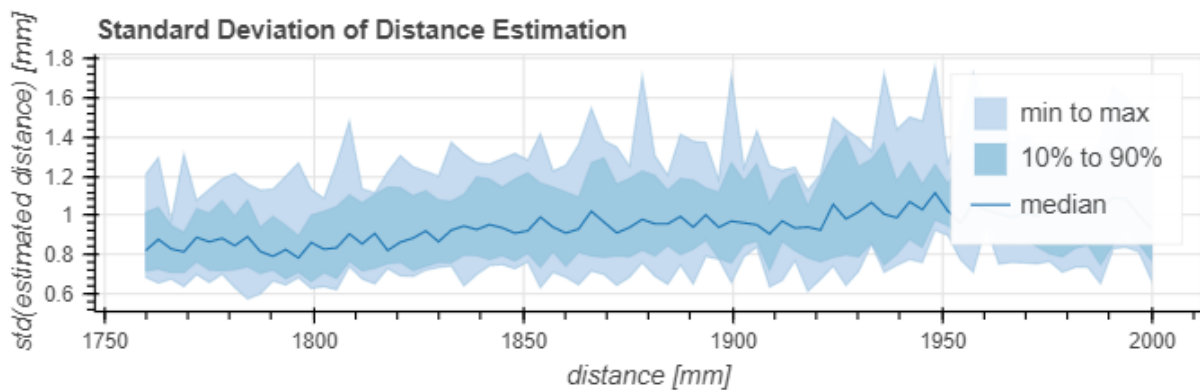
Figure 6.2. Standard deviation of distance estimation, maximize on SNR 1.76-2.0 m

6.2 Amplitude Accuracy

Conditions: T_A = 25 ℃, V_{DD} = 1.8 V. Statistical result based on sweep count 100, 20 tested devices.

The below figure shows the standard deviation of amplitude estimation, configuration with maximize on depth resolution used, 0.06-0.30 m. Object metal cylinder 40 mm diameter.
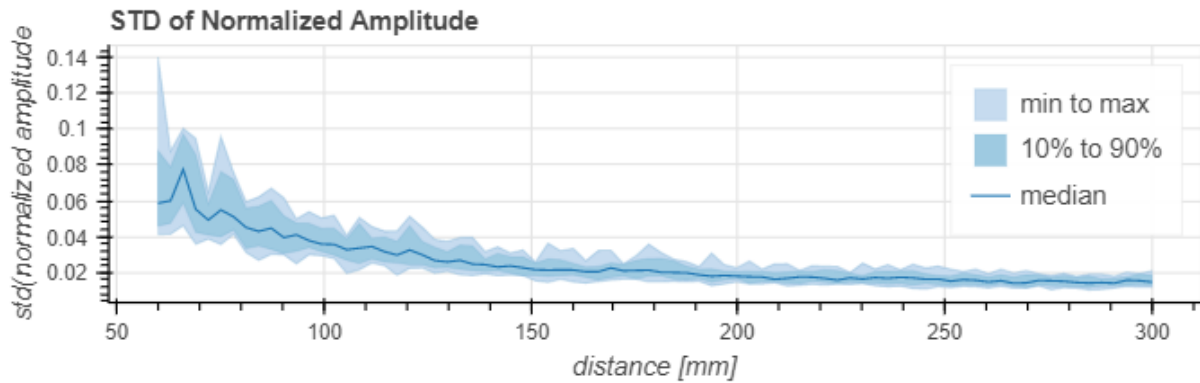

Figure 6.3. Standard deviation of amplitude estimation, maximize on depth resolution 0.06-0.30 m.

The below figure shows the standard deviation of amplitude estimation, configuration with maximize on SNR used, 1.76-2.0 m. Object 5 cm radius spherical metal corner reflector.
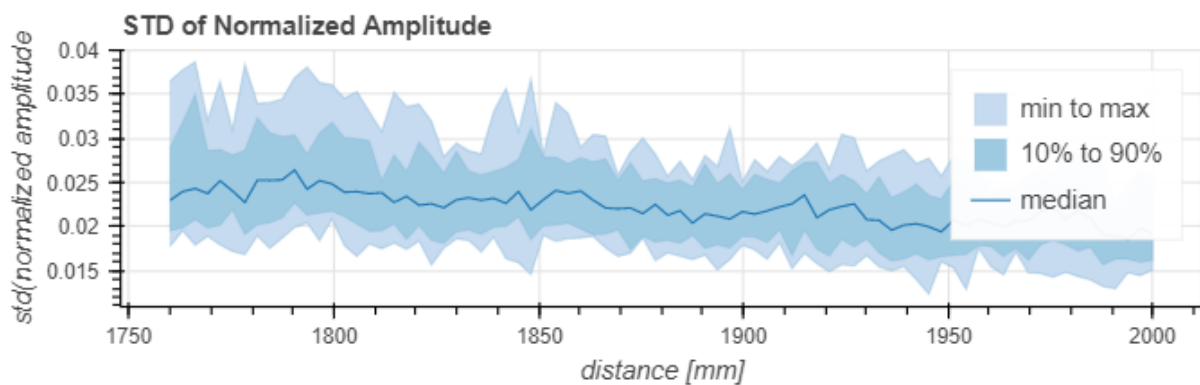

Figure 6.4. Standard deviation of amplitude estimation, maximize on SNR 1.76-2.0 m.

6.3 Relative Phase Accuracy

Conditions: T_A = 25 ℃, V_{DD} = 1.8 V. Statistical result based on sweep count 100, 20 tested devices.

Standard deviation of phase estimation, measured at a distance of 0.35 m. Object metal cylinder, 40 mm in diameter.

Average STD of relative phase estimation:

- 6.1 degrees in relative phase accuracy, translates to 42 µm in relative distance accuracy.

6.4 Half Power Beamwidth (HPBW)

Conditions: $T_A = 25$ ℃, $V_{DD} = 1.8$ V. Statistical result based on sweep count 100 (20 tested devices).

This section shows the A111 Elevation plane (E-plane) and Horizontal plane (H-plane) radiation pattern.

The below figure shows the normalized radiation pattern at E-plane, configuration with maximize on depth resolution used, with a 5 cm radius spherical metal corner reflector. HPBW for E-plane is ±20 degrees, as shown in the below figure.
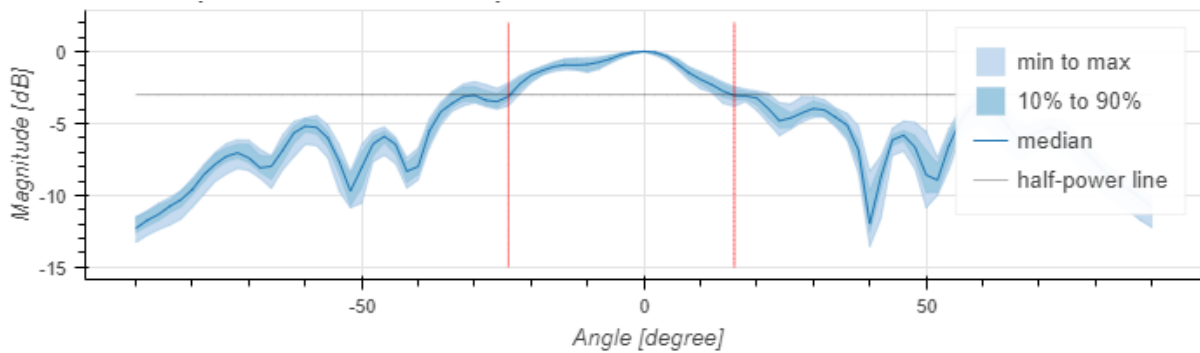

Figure 6.5. Normalized radiation pattern at E-plane.

The below figure shows the normalized radiation pattern at H-plane, configuration with maximize on depth resolution used, with a 5 cm radius spherical metal corner reflector. The HPBW for H-plane is ±40 degrees, as shown in the below figure.
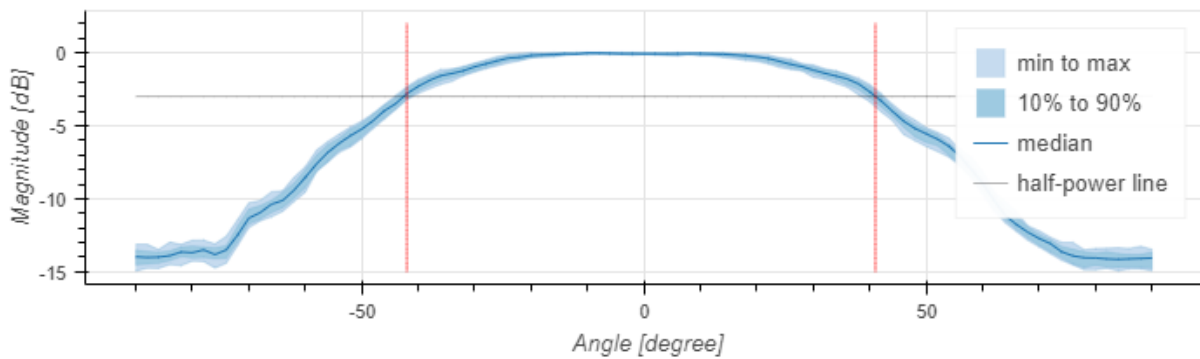

Figure 6.6. Normalized radiation pattern at H-plane

7 Functional Description

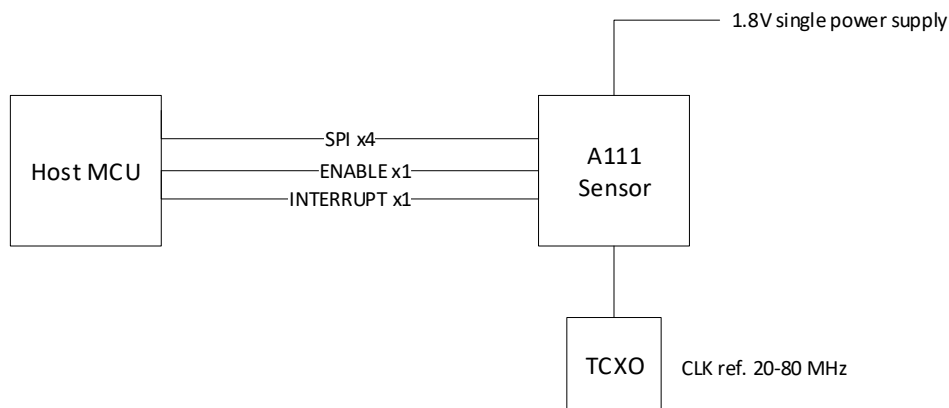The below figure shows the A111 system integration with Host MCU:

Figure 7.1. System integration

The Acconeer software is executed on Host MCU that handles sensor initiation, configuration, sweep acquisition and signal processing.

The Serial Peripheral Interface (SPI) is a 4-wire serial bus, used for configuration and reading output from the A111 radar sensor. The A111 radar sensor is an SPI slave device, connected to the SPI master (Host MCU), and allows several devices to be connected on same SPI bus, with a dedicated slave-select signal. Daisy-chain is not supported.

The sensor provides support for ENABLE and INTERRUPT as interrupt signal, always output, that can be used as an interrupt in the Host MCU.

7.1 Software Architecture

The Acconeer software has been written in C and is portable to any OS and HW platform. The Acconeer software is executed on Host MCU and delivered as binaries, except for driver software that is delivered as source code. The Acconeer software also provides example applications as reference source code for utilizing various Acconeer Services and Detectors, to facilitate customer software development on application level. Acconeer Services provides data and Acconeer Detectors provides result based on Service data.

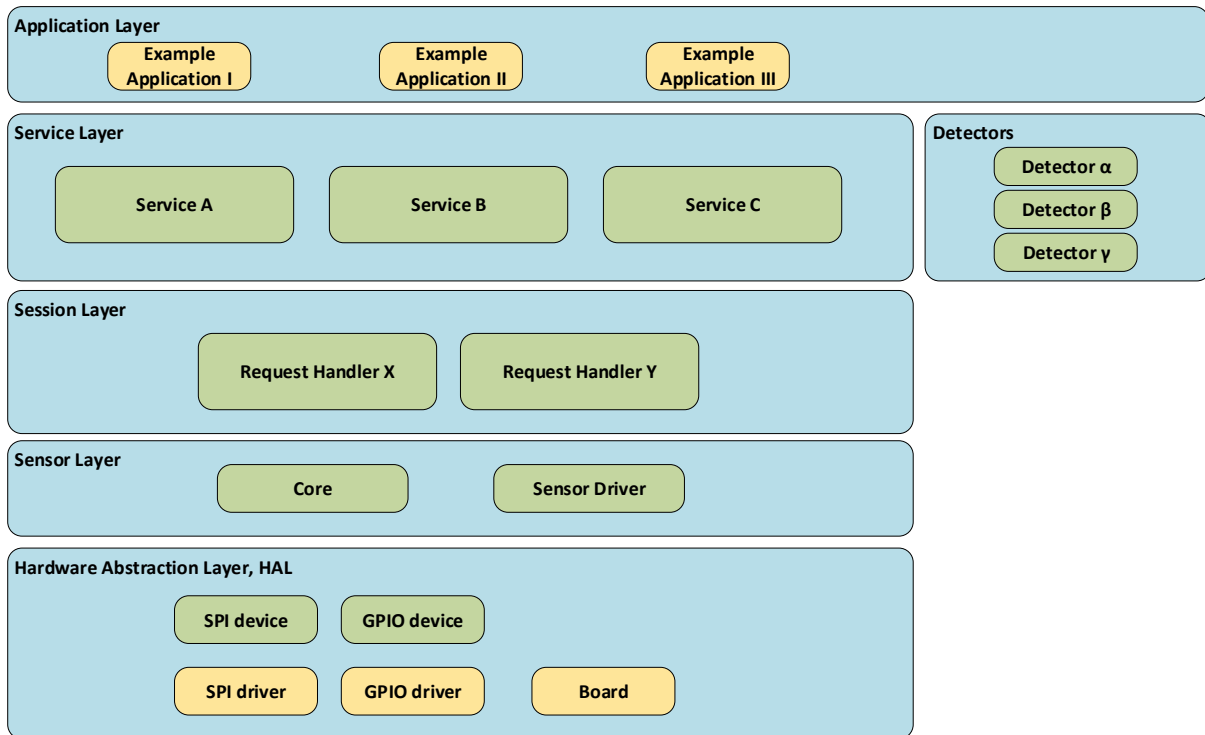The below figure shows the A111 software architecture:

Figure 7.2. SW architecture

Note: The green boxes are binaries and the yellow boxes are delivered as source code.

The Application layer addresses functional requests for various provided services using an Acconeer defined API (Application Programming Interface). Acconeer provides several example applications, that are service oriented. Also, customer guidelines are provided for application development utilizing the Acconeer API.

The Service layer handles functional requests on services and returns service data per request. The service data can be either processed by application itself or pushed from the application toward a specific detector to generate calculated result e.g. distance, amplitude.

The Session layer, depending on given service, creates dedicated sessions for one or multiple sensors. Note that multiple sensors are supported and handled from a single host, where the Acconeer software is running. A session is implemented by a request handler(s), handling sensor initiation, configuration, sweep acquisition and signal processing. Results are available through callback function or blocking function call.

The Sensor layer handles the sensor control and communication functions. Core function handles different sweep configurations, set in the API.

The HAL layer (Hardware Abstraction Layer) handles integration towards customer hardware, e.g. driver registration and pin mapping toward SPI and INTERRUPT. Acconeer provides several reference drivers as source code, e.g. Support for Cortex M4, Cortex M7 MCU's.

Acconeer also provides detectors, such as a distance detector where the application can push service data to retrieve data result.

7.2 Devices and Drivers

The driver for SPI and INTERRUPT shall implement the defined functions found in the corresponding device header file, acc_device_spi.h and acc_device_gpio.h. Registration of these functions shall be done in the acc_board_init function, see chapter 7.3 for details.

7.3 Board File Interface and Implementation

The board header file, acc_board.h is the board file interface. Contents may not be changed, implementation needed for all functions and parameters in the file. NOTE, an implementation may in some cases be empty.

A detailed description of each board file function is shown in the table below.

acc_board function	Description
acc_board_init	- Init - Register driver: SPI mandatory
acc_board_gpio_init	- Initiation of GPIO. - Mandatory pin for sensor operation is ENABLE
acc_board_start_sensor	- Start a sensor - Fulfill power up sequence
acc_board_stop_sensor	- Stop a sensor - Fulfill power down sequence
acc_board_get_spi_bus_cs	Get SPI bus number and chip select pin(s)
acc_board_chip_select	Custom chip select logic, empty implementation allowed
acc_board_is_sensor_interrupt_connected	Get interrupt connection status
acc_board_is_sensor_interrupt_active	Get interrupt status
acc_board_get_sensor_count	Sensor count, shall equal the number of possible sensors on the hardware setup
acc_board_get_ref_freq	Get the reference frequency to the sensor
acc_board_get_spi_speed	Get SPI speed
acc_board_set_ref_freq	Not used, empty implementation allowed

Table 7.1. Board file implementation

7.4 Power Up Sequence

The power-up sequence is described using the recommended integration shown in the below figure:
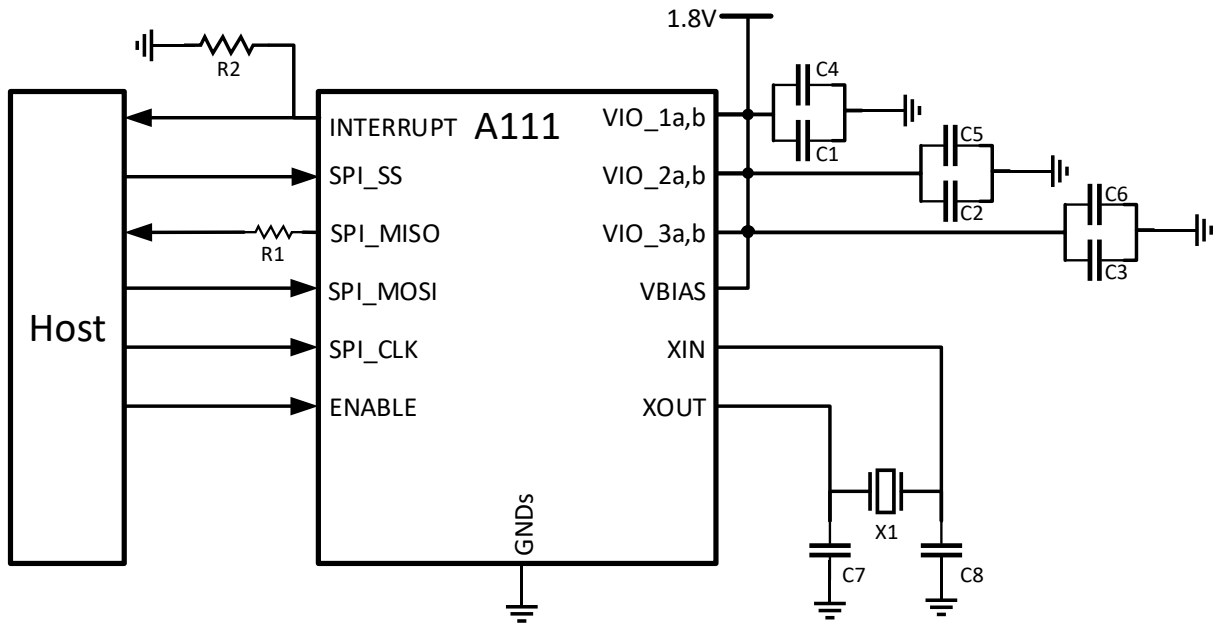

Figure 7.3. Recommended integration of the A111 radar sensor.

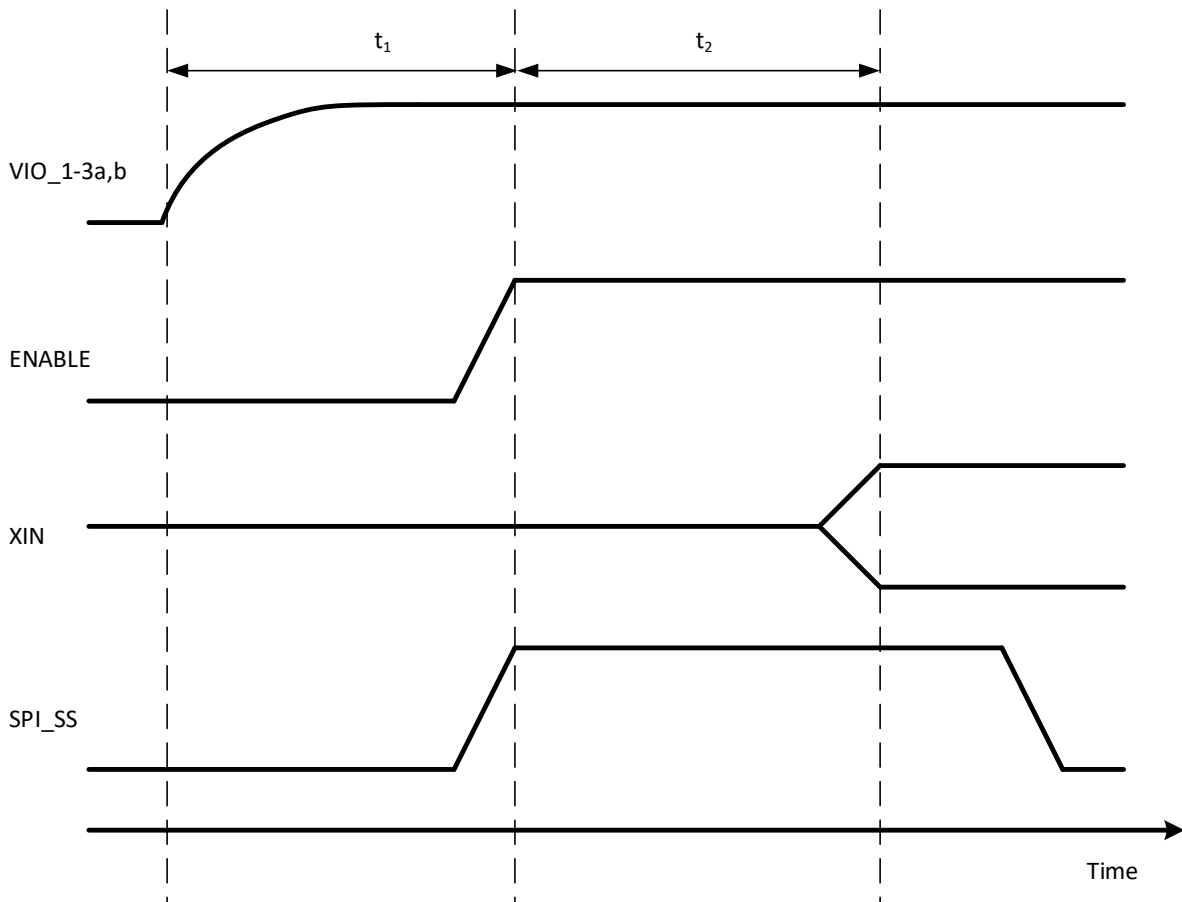The power up sequence is shown in below figure.

Figure 7.4. Power up sequence

It is recommended to allow the supply voltage on the sensor to stabilize before activating ENABLE. That is shown as the time t_1 in figure 7.4 and the actual time depends on the power supply and the value of the decoupling capacitors.

Next step in the power up sequence is to have a settling time for the XTAL oscillator to stabilize, shown as time t_2 in figure 7.4. This may take up to several milliseconds depending on the XTAL performance. The sensor does not require any settling time if it is integrated using an external reference clock. It is advised to have the clock inactive at 0 V while ENABLE is inactive.

Now the A111 radar sensor is ready for SPI communication. All I/Os must never exceed VIO_3 voltage.

After power up is complete, the sensor is loaded with a program. Up until the point where the sensor's program is started, the INTERRUPT pin is high impedance. However, after the sensor's program has started the INTERRUPT pin is configured to a push-pull CMOS output. Therefore it is required that the host I/O is configured as input before any programs are started on the sensor.

The power down sequence is recommended to be executed in the reverse order as the power up sequence: First ensure that all I/O inputs are at 0V which includes ENABLE, after that all VIO1_3a,b can be turned off.

VIO_1 and VIO_2 must never have higher voltage than VIO_3, and it is recommended to enable/disable the three supplies simultaneously.

External clock reference, if used, needs always to be available to sensor.

8   Layout Recommendations

A111 sensor free space integration should take the following into consideration:

- Any material above the sensor should have as low permittivity and loss as possible, e.g. plastic or glass with low permittivity.
- To conclude on optimum distance from the sensor, a simulation/measurement investigation is required.

The sensor antennas are of a folded dipole type, with its ground reference in the package ground plane, extending over the whole area of the sensor. To further enhance the directivity of the sensor, the package ground plane should be extended to the package by soldering all GND pins of the sensor to the board top layer ground. This top layer ground plane below the sensor should be continuous and should have low impedance.

The below table shows the sensor gain loss versus solid ground plane area.

Ground plane area	Sensor gain loss
625 mm^2	0 dB
425 mm2	-0.2 dB
225 mm^2	-0.4 dB
127 mm^2	-2.2 dB
29 mm^2	-4.0 dB

Table 8.1 Simulated relative maximum gain as function of extended solid ground plane area. The area is quadratic.

It is recommended to keep the layout around XIN and XOUT symmetrical to the XTAL and capacitors.

VIO_1a and VIO_1b are short circuit inside the sensor and are recommended to be connected to each other on the PCB as well. VIO_2a and VIO_2b are short circuit inside the sensor and are recommended to be connected to each other on the PCB as well. VIO_3a and VIO_3b are short circuit inside the sensor and are recommended to be connected to each other on the PCB as well. It is recommended to have decoupling capacitors on the supplies placed as close as possible to the supply terminals. It is recommended as minimum 100 nF in parallel with 1 uF decoupling capacitance on each supply.

The below table shows BOM for integration of the A111:

Component	Value	Description
C1, C2, C3	100 nF	VIO_1, VIO_2, VIO_3 decoupling
C4, C5, C6	1 µF	VIO_1, VIO_2, VIO_3 decoupling
R2	100 kΩ	INTERRUPT pull down resistor
R1	30 Ω	SPI_MISO series resistance (optional)
X1		XTAL 24 MHz, Epson TSX-3225 (optional)
C7, C8	8 pF [1]	XTAL freq. tuning capacitor (optional)

Table 8.2 BOM list

(1) See details in chapter 7.1 XTAL for C7, C8 value calculation.

See figure 7.3 that shows the optional XTAL populated.

2018-06-25

8.1 XTAL

The input clock can origin from a crystal (XTAL), connected to XIN and XOUT.

The A111 sensor has a built-in XTAL oscillator and by adding an external XTAL component, as shown the below figure 8.1, a reference design without any external clock reference supplied is possible. Note however, that the external clock reference still is supported and if used instead of an external XTAL, it is connected to XIN pin.
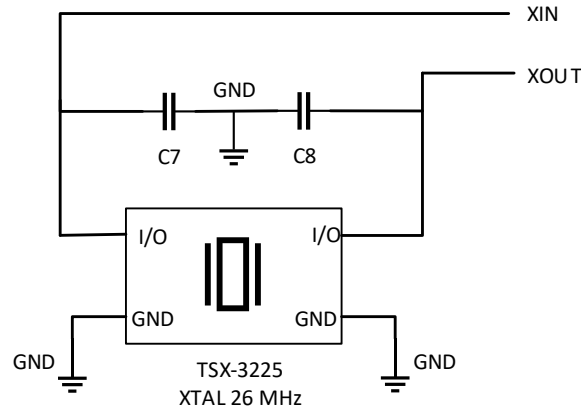

Figure 8.1. External XTAL schematics.

To enable the internal XTAL oscillator to drive the external resonator, the relation in equation 1 must be fulfilled.

Equation 1

$$f * C_{pin}^{0.8} * R_{ESR}^{0.61} < 0.7$$

Equation 2

$$C = 2(C_L - C_{stray})$$

Equation 3

$$C_{pin} = C + C_{stray}/2$$

The capacitance values are calculated in equation 2. C_L and R_{ESR} are XTAL parameters and vary from XTAL to XTAL. The stray capacitance is the sum of the capacitance between XIN and XOUT, which are found in the traces on PCB and in the package; 2 to 5 pF is a general estimation.

Example:

- f = 26 MHz
- C_L = 9 pF
- R_{ESR} = 40 ohm

Assuming that C_{stray} = 5 pF gives C7, C8 = 8 pF and that the condition is met with the result 0.41 < 0.7.

8.2 External clock source

The input clock can origin from an external clock source connected to XIN, with XOUT left open.

As an example given in table 8.3, maximum phase noise figures are given using 40 MHz external clock reference.

Offset frequency (Hz)	Min.	Typ.	Max.	Unit
1000			-80	dBc/Hz
10 000			-100	dBc/Hz
100 000			-120	dBc/Hz
1 000 000			-140	dBc/Hz
10 000 000			-155	dBc/Hz

Table 8.3: Phase noise using 40 MHz external clock reference

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9   Mechanical Data

The A111 is available in fcCSP package for mounting on a substrate. The below table shows mechanical data:

Parameter	Min.	Typ.	Max	Unit
Body X	5.15	5.20	5.25	mm
Body Y	5.45	5.50	5.55	mm
Body Z (height)		0.821	0.899	mm
Pitch	0.45	0.50	0.55	mm
Pin diameter	0.25	0.30	0.35	mm
Pin height	0.15	0.24		mm
Ball count		50		mm

Table 9.1. Mechanical data
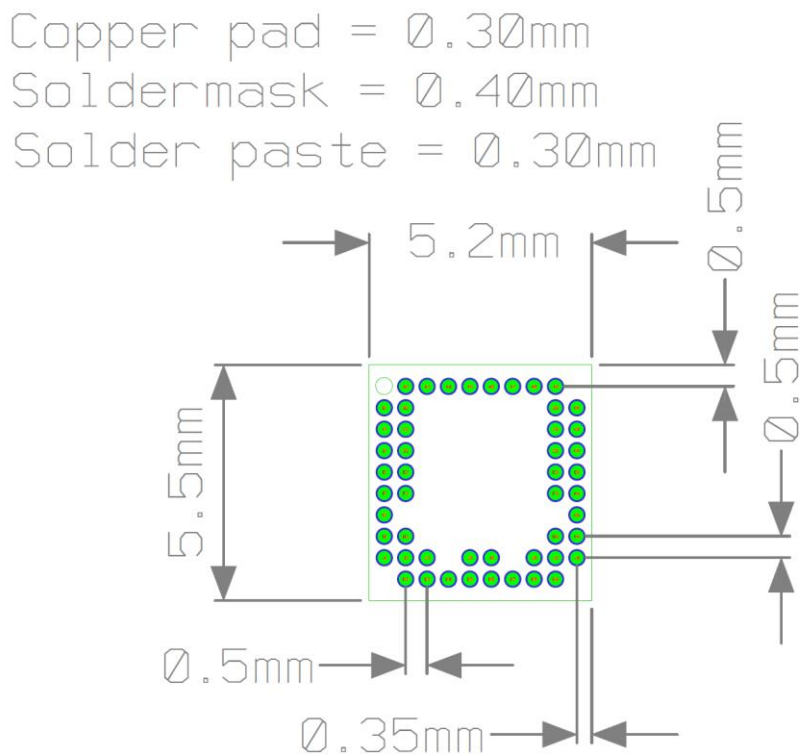
The A111 footprint is shown in Figure 9.1.

Figure 9.1. A111 footprint

The physical layout of the A111 sensor is shown in Figure 9.2, 9.3 and 9.4.
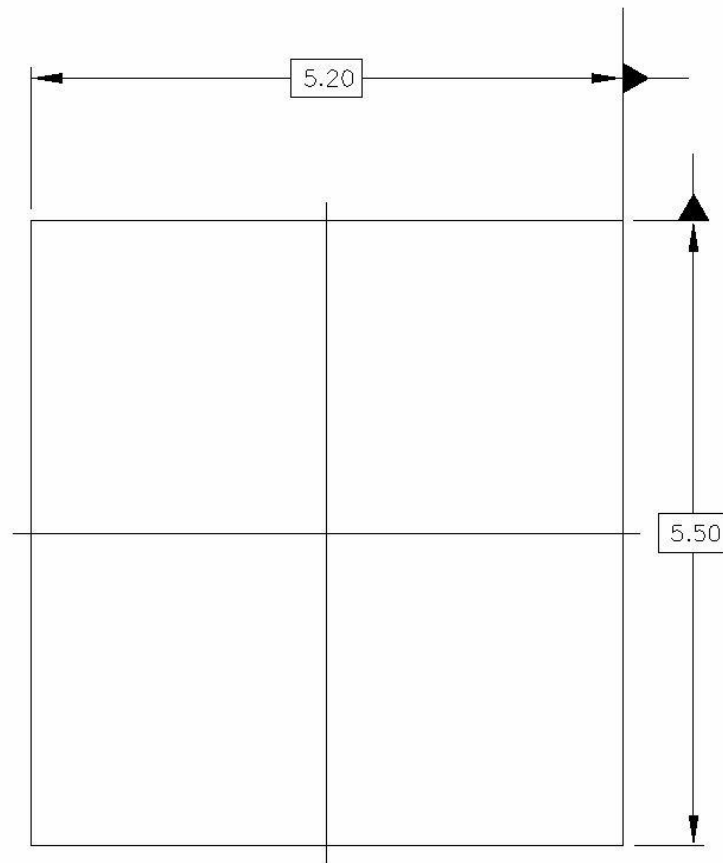

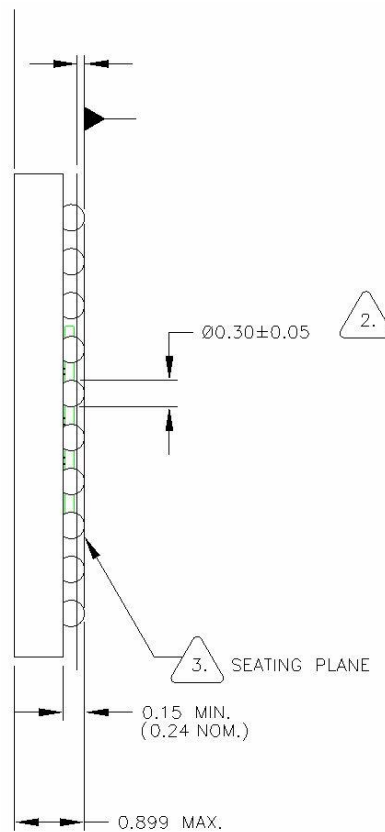*Figure 9.2. Physical layout of the A111 sensor, top view.*

Figure 9.3. Physical layout of the A111 sensor, side view.

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Primary datum C and seating plane are defined by the spherical crowns of the solder pins. Dimension is measured at the maximum solder pin diameter, parallel to primary datum C. All dimensions and tolerances conform to ASME Y14.5 – 2009.
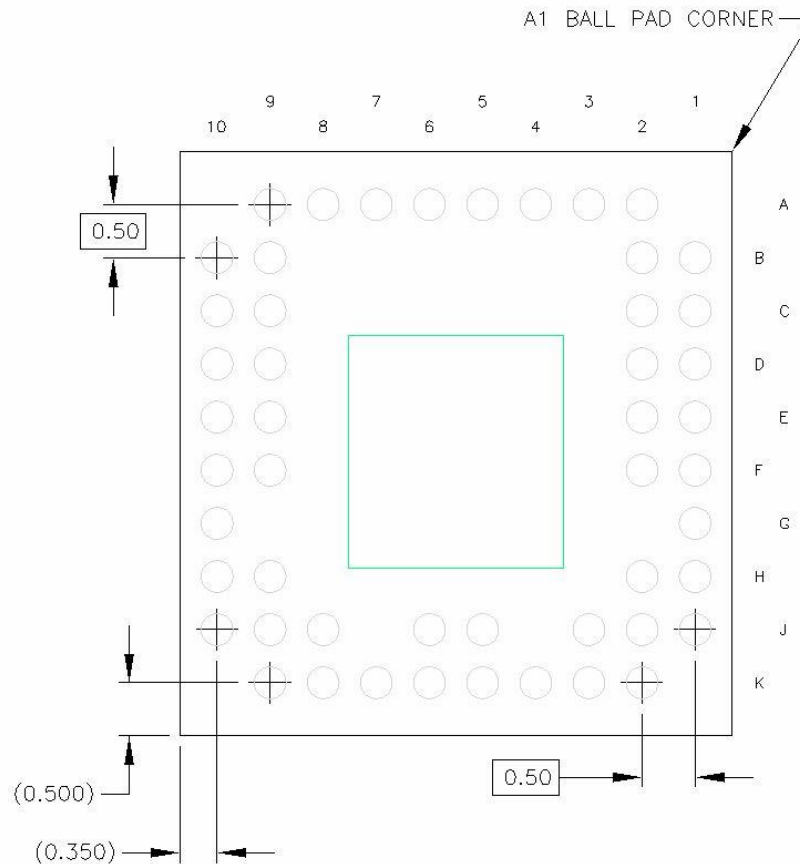

Figure 9.4. Physical layout of the A111 sensor, bottom view.

The bottom view shows 50 solder pins. The pitch of the BGA pins is 500 µm, the pin diameter is 300 µm ±5 µm and the collapsed pin height is 0.244 ± 0.050 mm.

9.1 Recommended Reflow Profile

Reflow Profiles per JEDEC J-STD-020.

10 Abbreviations

ADC	Analog digital converter
AiP	Antenna in package
API	Application programming interface
BGA	Ball grid array
BOM	Bill of materials
CPHA	Clock phase
CPOL	Clock polarity
EIRP	Equivalent isotropically radiated power
ESD	Electrostatic discharge
fcCSP	Flip-chip chip-scale package
GND	Ground
HAL	Hardware abstraction layer
HPBW	Half power beamwidth
LDO	Low-dropout regulator
MCU	Microcontroller unit
MISO	Master input, slave output
MOSI	Master output, slave input
NC	No connect
PCR	Pulse coherent radar
PLL	Phase locked loop
PoR	Power on reset
RCS	Radar cross section
RF	Radio frequency
RX	Receiver
SPI	Serial peripheral interface
SS	Slave select
STD	Standard deviation
TCXO	Temperature compensated crystal oscillator
TX	Transceiver
XTAL	Crystal

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