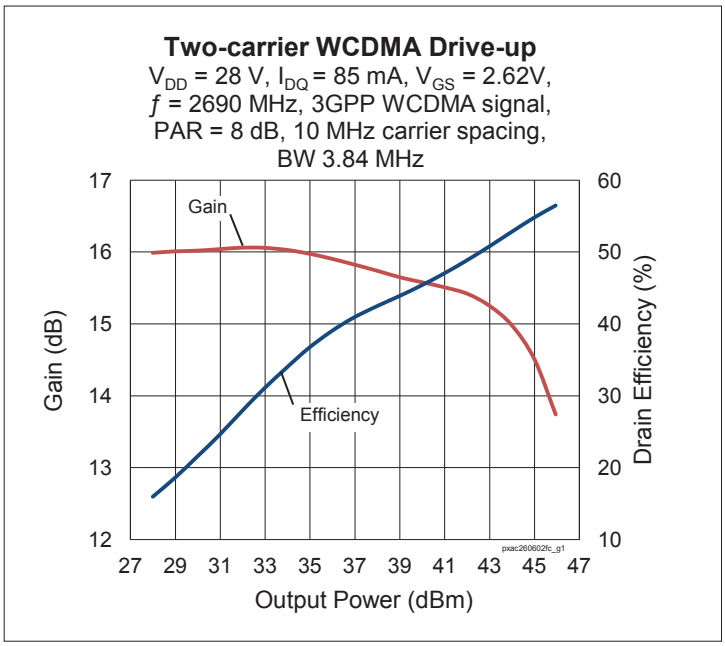
PXAC260602FC

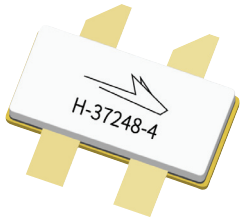
Thermally-Enhanced High Power RF LDMOS FET
60 W, P_{3dB} @ 28 V, 2620 – 2690 MHz

Description

The PXAC260602FC is a 60-watt LDMOS FET with an asymmetrical design intended for use in multi-standard cellular power amplifier applications in the 2620 to 2690 MHz frequency band. Features include dual-path design, high gain and thermally-enhanced package with earless flanges. Manufactured with Wolfspeed's advanced LDMOS process, this device provides excellent thermal performance and superior reliability.



PXAC260602FC
Package H-37248-4



Features

- Main: Input matched
  Peak: Input and output matching
- Asymmetric Doherty design
  - Main: P1dB = 15 W Typ
  - Peak: P1dB = 50 W Typ
- Typical Pulsed CW performance, 2690 MHz, 28 V, 10 µs pulse width, 10% duty cycle, class AB, Doherty Configuration
  - Output power at P_{1dB} = 50 W
  - Efficiency = 50%
  - Gain = 15 dB
- Typical two-carrier WCDMA performance, 2690 MHz, 28 V, 8 dB PAR @ 0.01% CCDF, Doherty Configuration
  - Output power = 5 W
  - Efficiency = 40%
  - Gain = 15.7 dB
  - IMD = –30 dBc
- Capable of handling 10:1 VSWR @28 V, 50 W (CW) output power
- Integrated ESD protection : Human Body Model, Class 1B (per JESD22-A114)
- Low thermal resistance
- Pb-free and RoHS compliant

RF Characteristics

Single-carrier WCDMA Specifications (tested in Wolfspeed Doherty test fixture)
V_{DD} = 28 V, I_{DQ} = 85 mA, P_{OUT} = 5 W avg, $V_{GS(PK)}$ = V_{GS} at 300 mA -1.0V, f = 2620 – 2690 MHz, 3GPP signal, channel bandwidth = 3.84 MHz, peak/average = 10 dB @ 0.01% CCDF

Characteristic	Symbol	Min	Typ	Max	Unit
Linear Gain	G_{ps}	14	15.7	—	dB
Drain Efficiency	η_D	35	39	—	%
Adjacent Channel Power Ratio	ACPR	—	–31	–28	dBc

All published data at T_{CASE} = 25°C unless otherwise indicated

ESD: Electrostatic discharge sensitive device—observe handling precautions!

DC Characteristics (each side)

Characteristic	Conditions	Symbol	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_{DS} = 10 mA	$V_{(BR)DSS}$	65	—	—	V
Drain Leakage Current	V_{DS} = 28 V, V_{GS} = 0 V	I_{DSS}	—	—	0.1	µA
	V_{DS} = 63 V, V_{GS} = 0 V	I_{DSS}	—	—	1.0	µA
Gate Leakage Current	V_{GS} = 10 V, I_{DS} = 0 V	I_{GSS}	—	—	—	µA
On-State Resistance (main)	V_{GS} = 10 V, V_{DS} = 0.1 V	$R_{DS(on)}$	—	0.8	—	Ω
(peak)	V_{GS} = 10 V, V_{DS} = 0.1 V	$R_{DS(on)}$	—	0.22	—	Ω
Operating Gate Voltage (main)	V_{DS} = 28 V, I_{DQ} = 85 mA	V_{GS}	2.5	2.75	3.0	V
(peak)	V_{DS} = 28 V, I_{DQ} = 300 mA	V_{GS}	2.3	2.7	3.1	V

Maximum Ratings

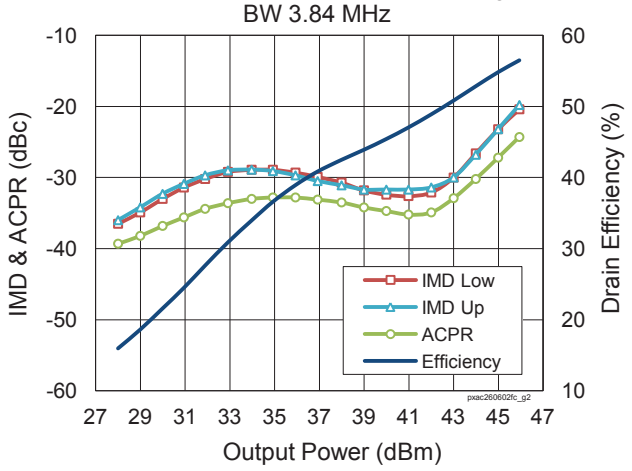
Parameter	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	65	V
Gate-Source Voltage	V_{GS}	–6 to +10	V
Operating Voltage	V_{DD}	0 to +32	V
Junction Temperature	T_J	225	°C
Storage Temperature Range	T_{STG}	–65 to +150	°C
Thermal Resistance (main, T_{CASE} = 70°C, 5 W CW)	$R_{\theta JC}$	4.1	°C/W
(doherty, T_{CASE} = 70°C, 20 W CW)	$R_{\theta JC}$	2.0	°C/W

Ordering Information

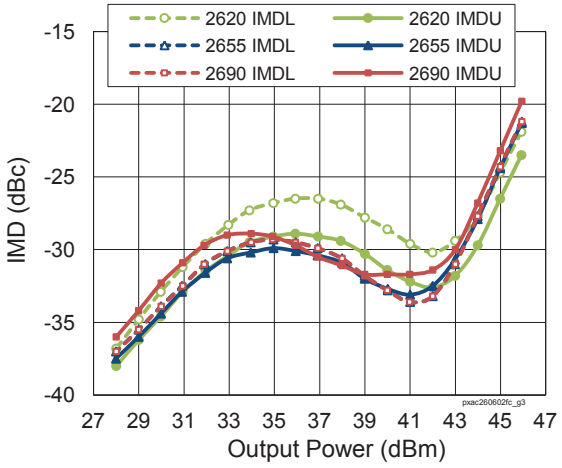
Type and Version	Order Code	Package Description	Shipping
PXAC260602FC V1 R0	PXAC260602FC-V1-R0	H-37248-4, earless flange	Tape & Reel, 50 pcs
PXAC260602FC V1 R250	PXAC260602FC-V1-R250	H-37248-4, earless flange	Tape & Reel, 250 pcs

Typical Performance (data taken in a production test fixture)

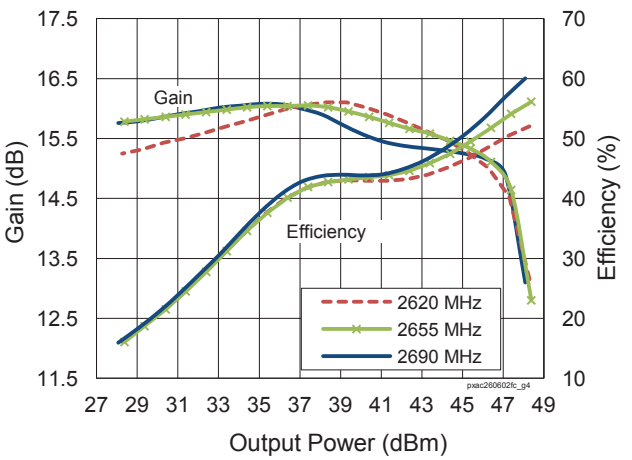
Two-carrier WCDMA Drive-up
V_{DD} = 28 V, I_{DQ} = 85 mA, V_{GS} = 2.62 V,
f = 2690 MHz, 3GPP WCDMA signal,
PAR = 8 dB, 10 MHz carrier spacing,
BW 3.84 MHz



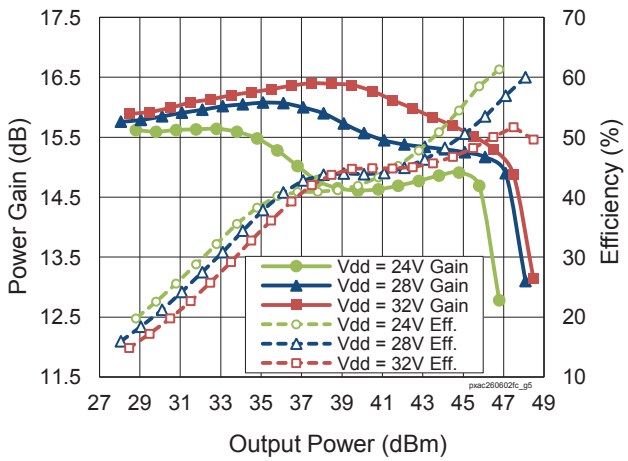
Two-carrier WCDMA Drive-up
V_{DD} = 28 V, I_{DQ} = 85 mA, V_{GS} = 2.62V,
3GPP WCDMA signal, PAR = 8 dB,
10 MHz carrier spacing, BW 3.84 MHz



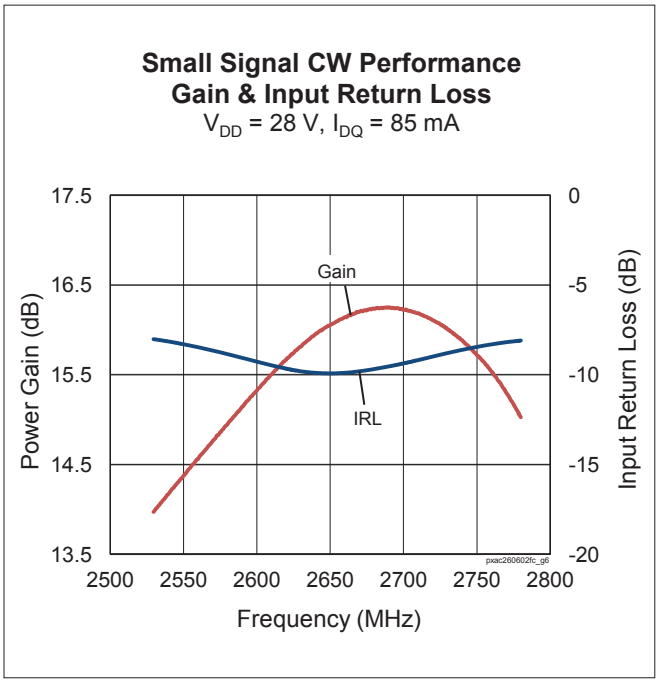
CW Performance
V_{DD} = 28 V, I_{DQ} = 85 mA



CW Performance
at various V_{DD}
I_{DQ} = 85 mA, f = 2690 MHz



Typical Performance (cont.)



Load Pull Performance

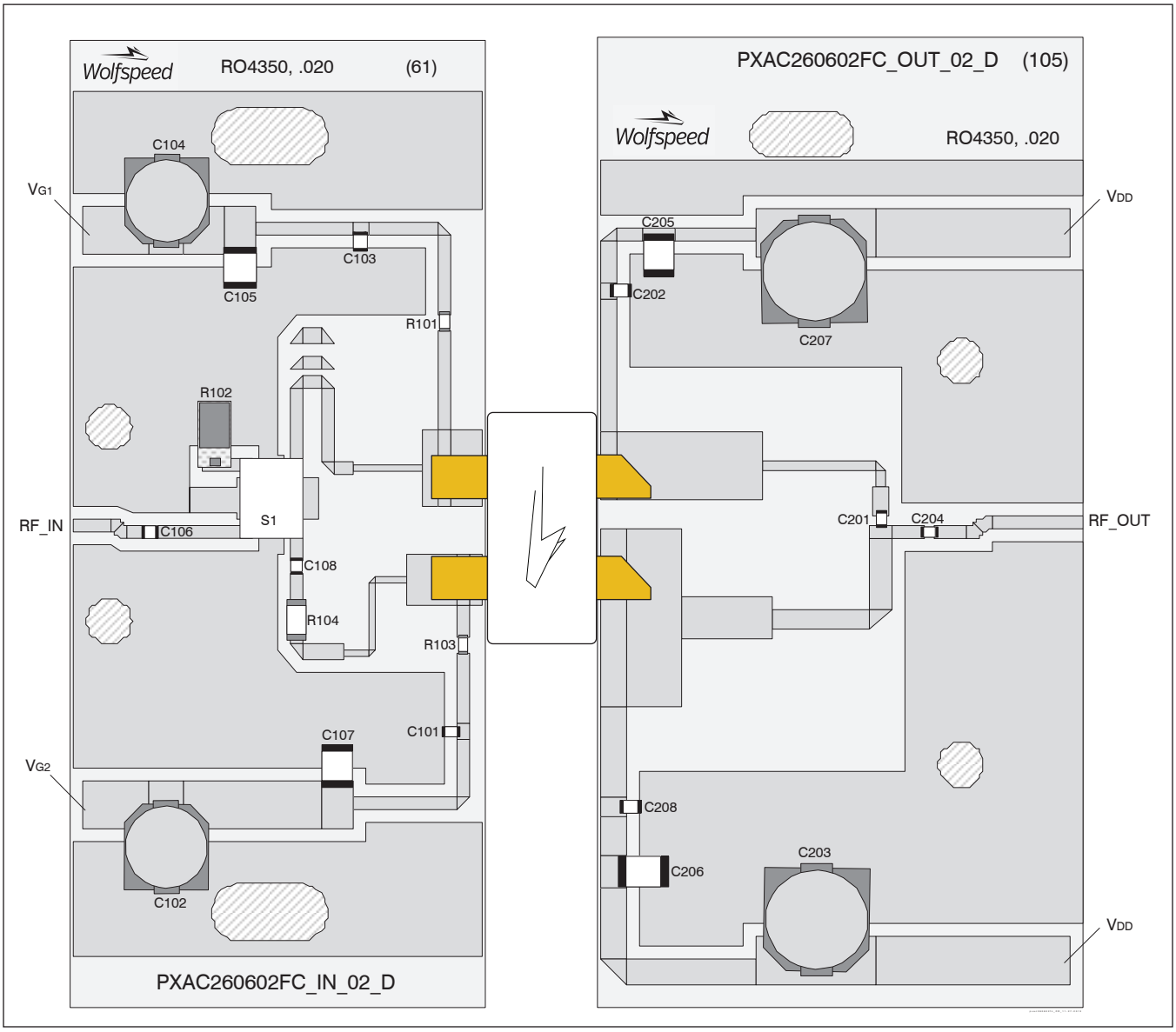
Main Side Load Pull Performance – Pulsed CW signal: 10 µs, 10% duty cycle, 28 V, 80 mA

		P_{1dB}									
		Max Output Power					Max PAE				
Freq [MHz]	Zs [Ω]	Zl [Ω]	Gain [dB]	P_{OUT} [dBm]	P_{OUT} [W]	PAE [%]	Zl [Ω]	Gain [dB]	P_{OUT} [dBm]	P_{OUT} [W]	PAE [%]
2490	9.0 – j33	12.8 – j9.5	19.2	42.84	19.2	54.2	5.8 – j4.4	21.9	41.49	14.1	68.7
2620	25 – j47	13.9 – j10.6	18.8	43.15	20.6	58.7	8.9 – j6.8	20.4	42.24	16.7	66.4
2690	35 – j52	12.7 – j13.0	18.6	42.76	18.9	55.4	6.8 – j9.2	20.6	41.73	14.9	65.6

Peak Side Load Pull Performance – Pulsed CW signal: 10 µs, 10% duty cycle, 28 V, 250 mA

		P_{1dB}									
		Max Output Power					Max PAE				
Freq [MHz]	Zs [Ω]	Zl [Ω]	Gain [dB]	P_{OUT} [dBm]	P_{OUT} [W]	PAE [%]	Zl [Ω]	Gain [dB]	P_{OUT} [dBm]	P_{OUT} [W]	PAE [%]
2490	4.1 – j13.1	3.7 – j5.2	16.7	48.44	70	56.0	6.2 – j1.3	18.9	46.59	46	63.4
2620	6.5 – j14.8	3.7 – j6.5	17	48.28	67	55.4	5.9 – j3.7	19.1	46.96	50	63.1
2690	9.0 – j17.8	3.7 – j6.1	17.6	48.11	65	56.2	5.7 – j2.4	20.9	46.30	43	64.6

Reference Circuit , 2620 – 2690 MHz



Reference circuit assembly diagram (not to scale)

Reference Circuit (cont.)

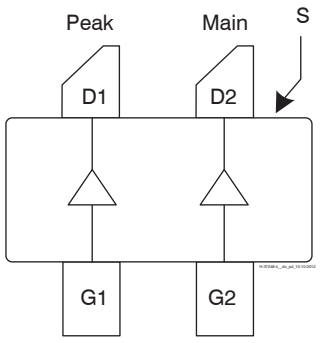
Reference Circuit Assembly

DUT	PXAC260602FC V1
Test Fixture Part No.	LTA/PXAC260602FC V1
PCB	Rogers 4350, 0.508 mm [0.020"] thick, 2 oz. copper, ε_r = 3.66, f = 2620 – 2690 MHz
Find Gerber files for this test fixture on the Wolfspeed Web site at www.wolfspeed.com/RF	

Components Information

Component	Description	Suggested Manufacturer	P/N
Input			
C101, C103, C106, C108	Capacitor, 18 pF	ATC	ATC800A180JT250T
C102, C104	Capacitor, 10 µF	Panasonic Electronic Components	EEE-HB1H100AP
C105, C107	Capacitor, 10 µF	Taiyo Yuden	UMK325C7106MM-T
R101, R103	Resistor, 10 Ω	Panasonic Electronic Components	ERJ-3GEYJ100V
R102	Resistor, 50 Ω	Anaren	C16A5024
R104	Resistor, 20 Ω	Panasonic Electronic Components	ERJ-8GEYJ200V
S1	Directional Coupler, 5dB	Anaren	X3C25P1-05S
Output			
C201, C202, C204, C208	Capacitor, 18 pF	ATC	ATC800A180JT250T
C203, C207	Capacitor, 100 µF	Panasonic Electronic Components	EEE-FP1V101AP
C205, C206	Capacitor, 10 µF	Taiyo Yuden	UMK325C7106MM-T

Pinout Diagram (top view)



Pin	Description
D1	Drain device 1 (Peak)
D2	Drain device 2 (Main)
G1	Gate device 1 (Peak)
G2	Gate device 2 (Main)
S	Source (flange)

Lead connections for PXAC260602FC

Package Outline Specifications

Package H-37248-4

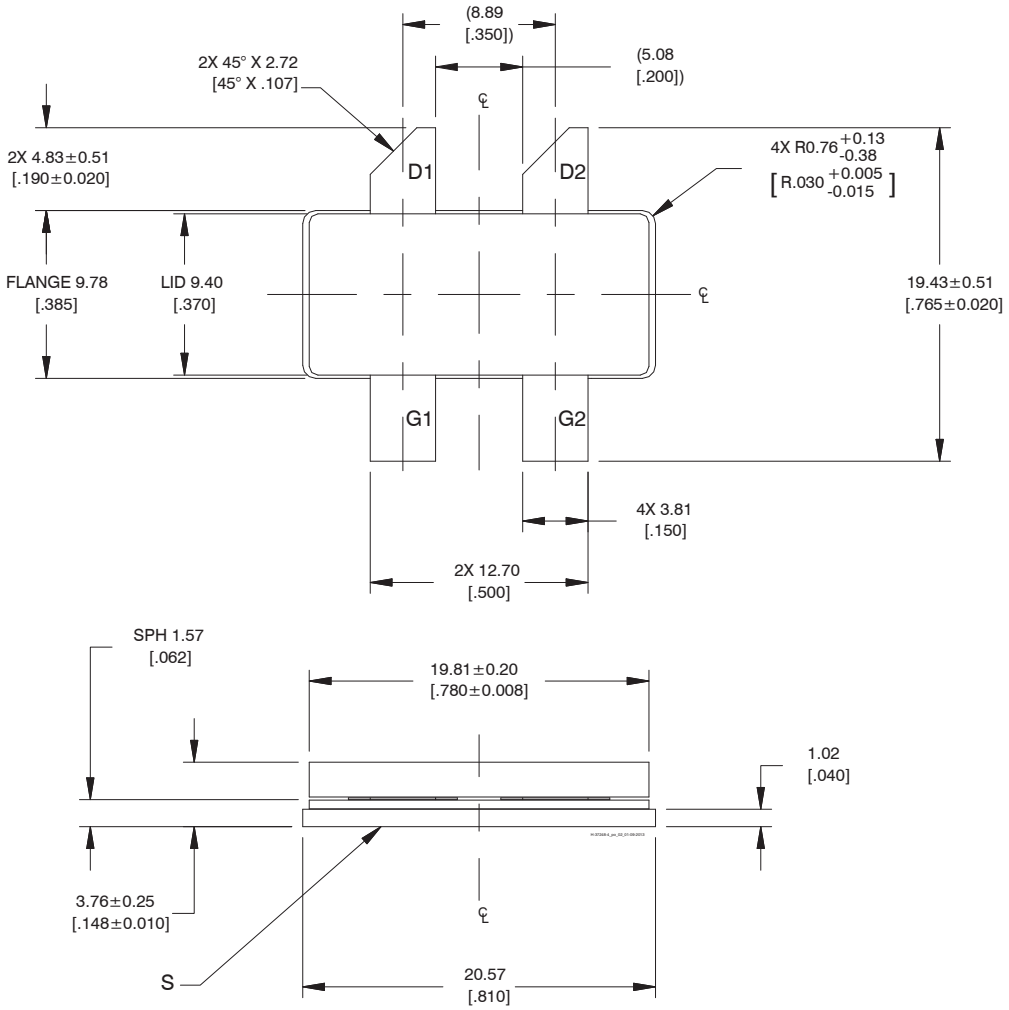


Diagram Notes—unless otherwise specified:

1. Interpret dimensions and tolerances per ASME Y14.5M-1994.
2. Primary dimensions are mm. Alternate dimensions are inches.
3. All tolerances ± 0.127 [.005] unless specified otherwise.
4. Pins: D1, D2 – drains; G1, G2 – gates; S – source.
5. Lead thickness: 0.10 + 0.076/–0.025 mm [0.004+0.003/–0.001 inch].
6. Gold plating thickness: 1.14 ± 0.38 micron [45 ± 15 microinch].

Revision History

Revision	Date	Data Sheet Type	Page	Subjects (major changes since last revision)
01	2013-10-14	Advance	All	Data Sheet reflects advance specification for product development
02	2013-12-02	Production	All	Data Sheet reflects released product specification
02.1	2013-12-12	Production	1	Revised ESD classification
02.2	2014-05-14	Production	2 6	Revised juntion temperature in Maximum Ratings table Corrected naming typo in Pinout Diagram
02.3	2015-12-23	Production	2	DC Characteristic table
02.4	2016-06-22	Production	2	Updated ordering information
03	2018-07-03	Production	All	Converted to Wolfspeed Data Sheet

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Notes

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